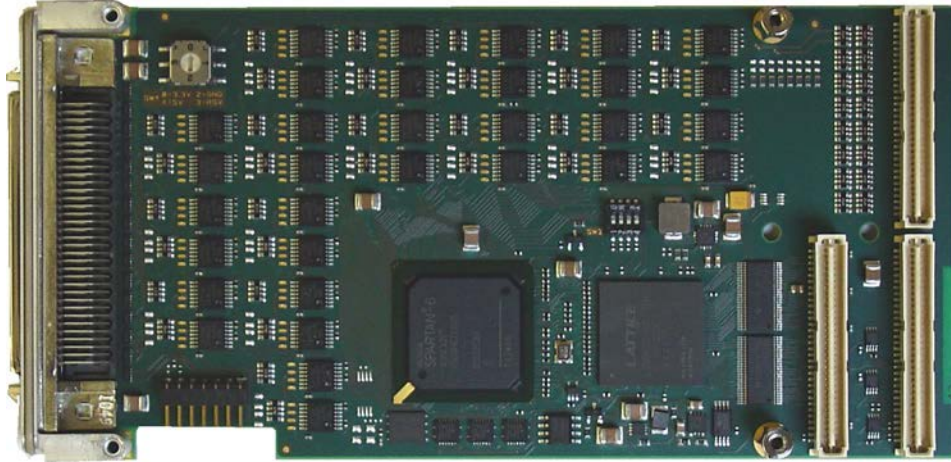# TEWS TECHNOLOGIES

The Embedded I/O Company

TPMC634   Re-Configurable FPGA with 64 TTL I/O / 32 Diff. I/O

Application Information

The TPMC634 is a standard single-width PMC module providing a user configurable Xilinx XC6SLX25 Spartan-6 FPGA.

The TPMC634-10R provides 64 ESD-protected TTL lines using TTL compatible buffers. The TPMC634-11R provides 32 differential I/O lines using ESD-protected EIA-422 / EIA-485 compatible line transceivers. The TPMC634-12R provides a mix of 32 TTL and 16 differential RS422/485 I/O lines. The TPMC634-13R provides 32 differential I/O lines using M-LVDS line transceivers. The TPMC634-14R provides a mix of 32 TTL and 16 differential M-LVDS I/O lines.

All I/O lines are individually programmable as input or output. The receivers are always enabled. This allows reading the state of each I/O line at any time (monitoring I/O lines configured as outputs).
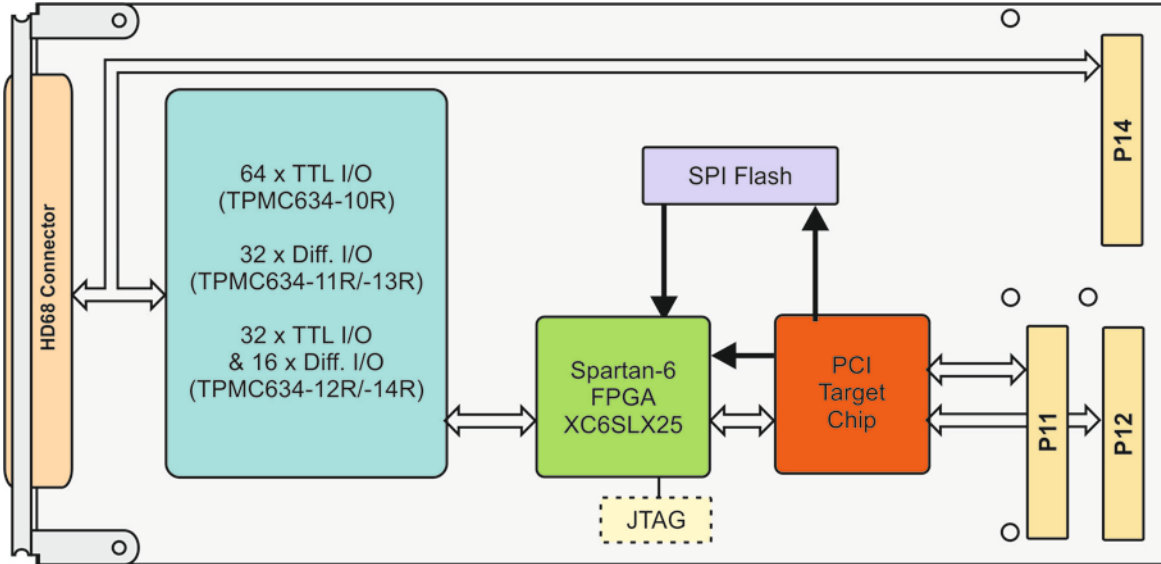
Each TTL I/O line has an on-board pull resistor to a common/shared reference. The pull resistor reference is configurable by an on-board rotary switch to 3.3V, 5V or GND. The differential I/O lines have on-board termination resistors.

The User FPGA is auto-configurable by an on-board serial SPI Flash. Both the User FPGA and the SPI flash for User FPGA configuration are in-system-programmable via the PCI bus. An on-board JTAG header provides access to the user FPGA JTAG port.

PCI configuration space parameters are configurable by an on-board serial EEPROM.

Technical Information

- Standard single-width 32 bit 33 MHz PCI PMC Module conforming to IEEE P1386.1
- PCI 3.0 compatible Interface
- Universal PCI Signaling Voltage
- Xilinx XC6SLX25 Spartan-6 User FPGA accessible on Local Address/Data Bus
- PCI to Local Bus Interface is handled by the PCI Target Chip
- Programmable EEPROM for PCI Configuration Space Parameters
- In-System-Programmable SPI Flash for User FPGA Configuration
- User FPGA directly In-System-Programmable by Software
- Baud Rate Oscillator available at User FPGA Pin
- I/O options:
  - 64 TTL I/O (-10R)
  - 32 differential I/O RS422/485 (-11R)
  - 32 TTL I/O and 16 diff. I/O RS422/485 (-12R)
  - 32 differential I/O M-LVDS (-13R)
  - 32 TTL I/O and 16 diff. I/O M-LVDS (-14R)
- 64 I/O lines accessible on both HD68 Front Connector and P14 Rear Connector
- Operating Temperature -40°C to +85°C

64 x TTL I/O
(TPMC634-10R)

32 x Diff. I/O
(TPMC634-11R/-13R)

32 x TTL I/O
& 16 x Diff. I/O
(TPMC634-12R/-14R)

HD68 Connector

SPI Flash

Spartan-6
FPGA
XC6SLX25

PCI
Target
Chip

JTAG

P14

P11

P12

Order Information

RoHS Compliant

TPMC634-10R   Re-Configurable FPGA with 64 TTL Inputs/Outputs
TPMC634-11R   Re-Configurable FPGA with 32 Differential RS422/485 Inputs/Outputs
TPMC634-12R   Re-Configurable FPGA with 32 TTL Inputs/Outputs and 16 Differential RS422/485 Inputs/Outputs
TPMC634-13R   Re-Configurable FPGA with 32 Differential M-LVDS Inputs/Outputs
TPMC634-14R   Re-Configurable FPGA with 32 TTL Inputs/Outputs and 16 Differential M-LVDS Inputs/Outputs

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TPMC634-DOC User Manual

Software

For Software Support please contact TEWS.

Related Products

TA304   Cable Kit for Modules with HD68 SCSI-3 type connector
TPIM003   PIM I/O Module with HD68 SCSI-3 type connector and special pin assignment