# AMC588

## 300 MHz to 6 GHz Octal Versatile Wideband Transceiver (MIMO), UltraScale+™ AMC

AMC588

## Key Features

- Xilinx UltraScale+™ XCVU13P FPGA
- Octo complete transceiver signal chain solution
- Based on quad Analog Devices AD9371
- Frequency range 300 MHz to 6 GHz
- Tx synthesis bandwidth (BW) to 250 MHz
- Rx bandwidth: 8 MHz to 100 MHz
- Supports Time Division Duplex (TDD) and Frequency Division Duplex (FDD) operation
- On-board clocking or external clock with multi-transceivers synchronization capability
- IPMI 2.0 compliant

## Benefits

- High density transceiver with intensive data processing capability
- Flexible clocking
- Observation channels for implementation of error correction functions
- Sniffer Receiver channels can monitor different frequency bands
- Xilinx UltraScale+™ XCVU13P FPGA provides powerful compute resource
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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# AMC588

The AMC588 is a wideband transceiver in AMC form factor. The AMC utilizes four AD9371 connected to a Virtex UltraScale+™ FPGA providing eight transceivers channels making it suitable for signal SDR, BTS, antenna systems, research and instrumentation.

The on-board re-configurable UltraScale+™ XCVU13P FPGA interfaces via JESD204B directly to wideband transceivers. The FPGA has interface to a single bank of DDR4 memory channels (64-bit wide for a total of 8 GB). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

*Figure 1: AMC588*

# Block Diagram

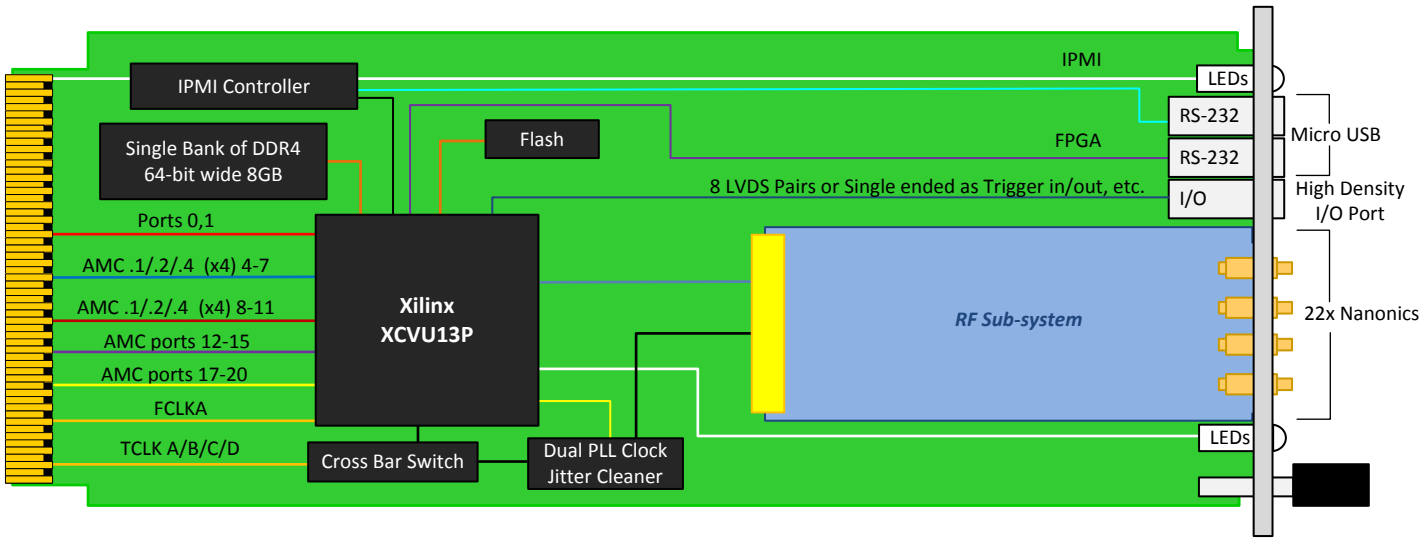



*Figure 2: AMC588 Functional Block Diagram*

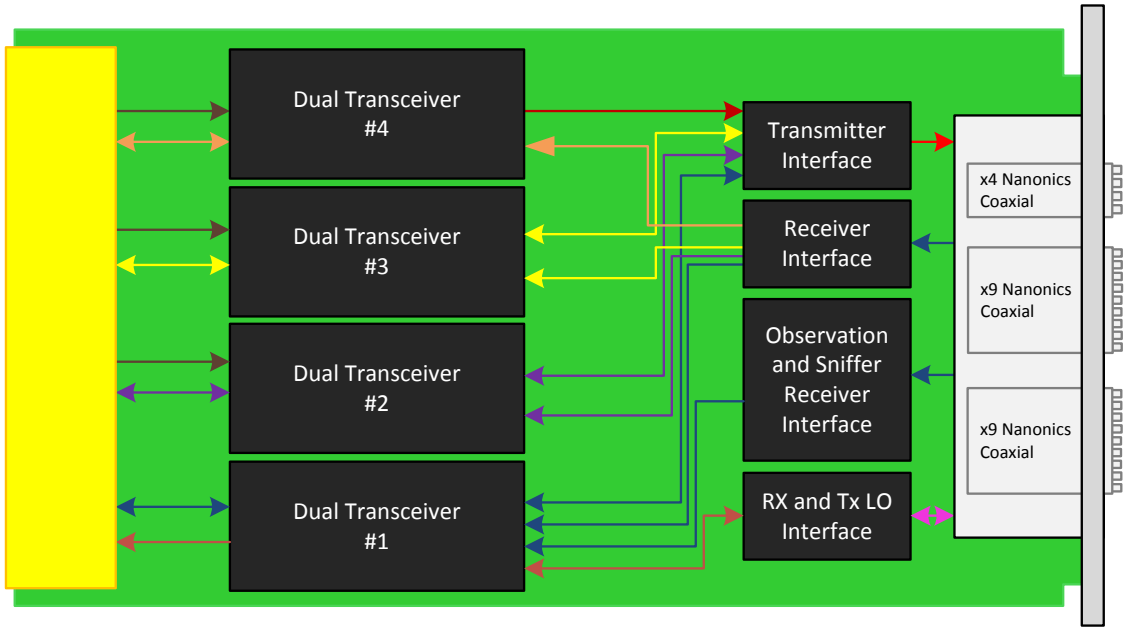



*Figure 3: AMC588 RF Sub-system*

# Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

# Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

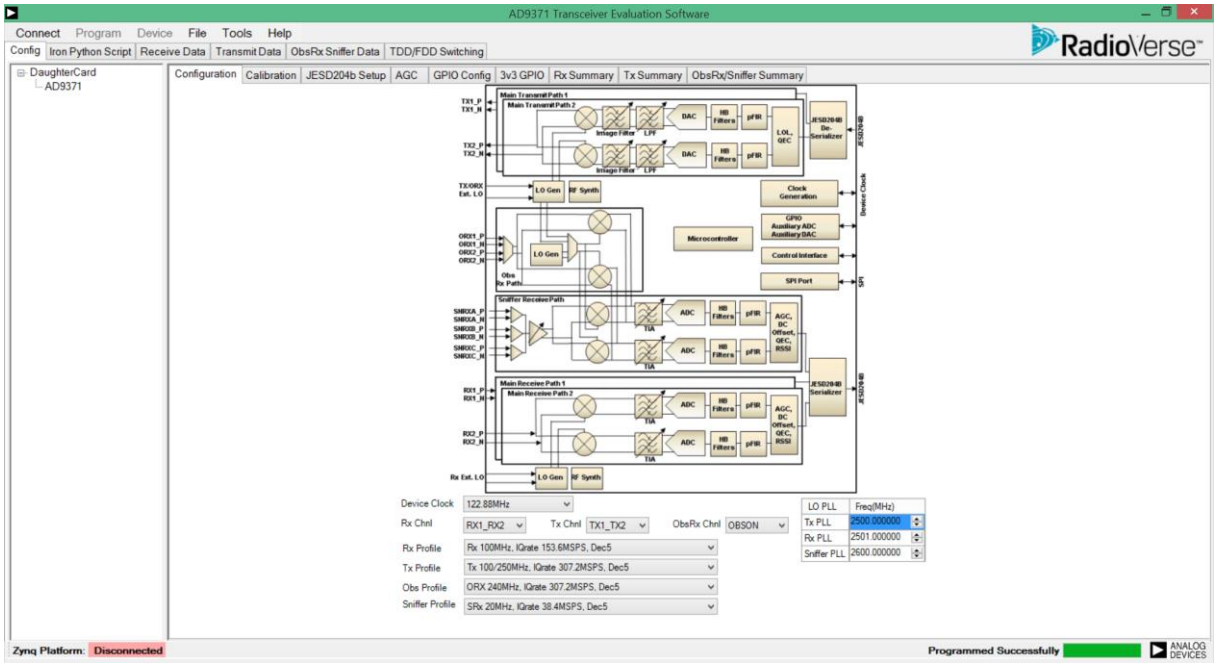
The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

The AMC588 is compatible with Analog Devices design tools for AD9371.



# Specifications

| | | |
|---|---|---|
| **Architecture** | | |
| **Physical** | **Dimensions** | Single module, 8 HP |
| | | Width: 2.89” (73.5 mm) |
| | | Depth: 7.11” (180.6 mm) |
| **Type** | **AMC FPGA ADC/DAC** | Xilinx UltraScale™ XCVU13P FPGA |
| | | Single bank of DDR4:64-bit, 8 GB |
| | | Octal wideband transceivers, AD9371 |
| **Standards** | | |
| **AMC** | **Type** | AMC.1, AMC.2 and AMC.4 (FPGA Programmable) |
| **Module Management** | **IPMI** | IPMI v2.0 |
| **PCIe** | **Lanes** | Single x4 or x8 via FPGA to AMC |
| **SRIO/XAUI** | **Lanes** | Single or Dual x4 via FPGA to AMC |
| **SerDes** | **Lanes** | x8 via FPGA to AMC ports 12-15 and 17-20 |
| **Ethernet** | **GbE and 10 GbE** | Dual GbE and 10/40 GbE |
| **Configuration** | | |
| **Power** | **AMC588** | ~70 W application dependent (may go up to 85 W) |
| **Environmental** | **Temperature** | See ordering options and environmental spec sheet |
| | | Storage Temperature: –40° to +85°C |
| | **Vibration** | Operating 9.8 m/s$^2$ (1 G), 5-500 Hz on each axis |
| | **Shock** | Operating 30 Gs each axis |
| | **Relative Humidity** | 5 to 95% non-condensing |
| **Front Panel** | **Interface Connectors** | 22x Nanonics Coaxial: 1x4 and 2x9 connectors |
| | | Micro USBs for MGT RS-232 and FPGA RS-232 |
| | | 1x mini Display Port |
| | **LEDs** | IPMI management control |
| | | 8 user defined LEDs |
| | **Mechanical** | Hot swap ejector handle |
| **Software Support** | **Operating System** | Agnostic |
| **Other** | | |
| **MTBF** | MIL Hand book 217-F@ TBD hrs | |
| **Certifications** | Designed to meet FCC, CE and UL certifications, where applicable | |
| **Standards** | VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards | |
| **Warranty** | Two (2) years | |

### INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

# Ordering Options

### AMC588 – A0C-0EF-G0J

| A = RF Direct Clock Sampling | | G = Clock Holdover Stability |
|---|---|---|
| 0 = Direct Clock<br>1 = On Board wide band PLL | | 0 = Standard (XO)<br>1 = Stratum-3 (TCXO) |
| | **E = FPGA Speed** | |
| | 1 = High (-2) *<br>2 = High (-2LE)<br>3 = Highest (-3E) * | |
| **C = Front Panel Size** | **F = PCIe Option **** | **J = Temperature Range and Coating** |
| 1 = Reserved<br>2 = Reserved<br>3 = Reserved<br>4 = Reserved<br>5 = Reserved<br>6 = Reserved<br>7 = 8 HP<br>8 = 8 HP, MTCA.1 (captive screw both side)<br>9 = 8 HP, SLF*** (captive screw one side) | 0 = No PCIe<br>1 = PCIe on ports 4 – 7<br>2 = PCIe on ports 8-11<br>3 = PCIe on ports 4 – 11<br>(x8 or dual x4 requires PCIe softcore for 8-11) | 0 = Commercial (–5° to +55°C), No coating<br>1 = Commercial (–5° to +55°C), Humiseal 1A33 Polyurethane<br>2 = Commercial (–5° to +55°C), Humiseal 1B31 Acrylic<br>3 = Industrial (–20° to +70°C), No coating<br>4 = Industrial (–20° to +70°C), Humiseal 1A33 Polyurethane<br>5 = Industrial (–20° to +70°C), Humiseal 1B31 Acrylic<br>6 = Extended (–40° to +85°C), Humiseal 1A33 Polyurethane ****<br>7 = Extended (–40° to +85°C), Humiseal 1B31 Acrylic **** |

Notes: *Minimum Order Quantity applies for these FPGA SKU's.
**When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.
*** Single Latch Flange (SLF)
****Conduction cooled, temperature is at edge of module.

# Related Products

VT951

MicroTCA rugged 1U 19" rackmount chassis platform

Designed to meet MIL-STD-810F, MIL-STD-901D for shock/vibration

Designed to meet MIL-STD-461E for EMI

FMC214

Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver

Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz

MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

AMC599

Xilinx UltraScale™ XCKU115 FPGA

Dual ADC @ 6.4 GSPS 12-bits or quad ADC at 3.2 GSPS

Dual DAC (AD9162 or AD9164) @ 12 GSPS, 16-bits

# Contact

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