µTCA 1U Chassis with 6 AMC slots with SFP+

VT842

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KEY FEATURES

- Six mid-height AMC slots per 1U Carrier or two double width mid-height with two mid-height AMC slots
- Cascade any number of 1U Carriers for Fabric expansion and management
- Management can run as Shelf/MCMC (MicroTCA Carrier Management Controller) or MCMC
- AMC.1, AMC.2, AMC.3, AMC.4 compliant
- PCIe, SRIO, 10GbE available on ports 4 to 7 and 8 to 11
- GbE Managed Layer Two (ports 0 and 1)
- Dual SFP+ for 10GbE
- Telco Alarm and Carrier Locator
- Telcom/GPS Clock on TCLKA, TCLKB, TCLKC and TCLKD and Fabric Clock on FCLK
- Redundant Cooling Units (CU)
- Removable Power Supply, Air Filter and Fan Trays
- IPMI 2.0 compliant
- RoHS compliant

The VT842 is a 1U µTCA chassis that provides six mid-height AMC slots that can accept any of the following Fabrics: PCIe, SRIO or 10GbE on ports 4 to 7 and 8 to 11, AMC.2 (ports 0 and 1) and AMC.3 (ports 2 and 3 are routed to adjacent slots). It provides FLCK, TCLKA, TCLKB, TCLKC and TCLKD to each AMC.

The VT842 has redundant Cooling Units. The Air Filter and Fan Trays are all hot swappable. The Power Entry Module (PEM) is removable for ease of serviceability.

The VT842 runs VadaTech proven second generation Management software based on it's VT002 product. The shelf manager implements IPMI management, FRU management, and shelf environment management for power, thermal, E-keying, etc. The VT002 can run as the Shelf/MCMC or MCMC.

The VT842 has dual SFP+ on the front panel when utilizing the 10GbE as a fabric.

The input power is from DC (-36V to -75V) or Universal AC.

µTCA™

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µTCA 1U Chassis with 6 AMC slots with SFP+

SPECIFICATIONS

Architecture		
		Height 1U
Physical	**Dimensions**	Width: 19”
		Depth 13” (330 mm)
Type	**AMC Carrier**	Six AMC.0 mid-height
Standards		
AMC	**Type**	AMC.1, AMC.2, AMC.3 and AMC.4
PCIe	**Lanes**	Each AMC slot may negotiate PCIe x1, x2, x4 or x8 lanes
SRIO	**Lanes**	Each AMC slot has two x4 (ports 4-7 and 8-11)
10GbE	**Lanes**	Each AMC slot has a dual XAUI interface (ports 4-7 and 8-11)
GbE	**1000-BX**	Two GbE SerDes per AMC (ports 0 and 1)
Telco Clk	**MLVDS**	Per AMC.0 specifications for TCLKA,TCLKB, TCLKC and TCLKD
Fabric Clk	**HCSL**	Per AMC.1 100 MHz HCSL
Module Management	**IPMI**	IPMI Version 2.0
Configuration		
Power	**VT842**	300W AC supply, 110-240VAC with frequency from 47-63Hz
		398W DC -36 to -75V
Environmental	**Temperature**	Operating Temperature: 0° to 55° C
		Storage Temperature: -40° to +90° C
	Vibration	0.5Gs RMS, 20-2000Hz random (Operating): 6Gs RMS (non-operating)
	Shock	30Gs each axis
	Relative Humidity	5 to 95 percent, non-condensing
Conformal Coating		Humiseal 1A33 Polyurethane
		Humiseal 1B31 Acrylic
Other		
MTBF	MIL Hand book 217-F@ TBD Hrs.	
Certifications	Designed to meet FCC, CE and UL certifications where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Compliance	RoHS and NEBS	
Warranty	Two (2) years	
Trademarks and Logos	The VadaTech logo is a registered trademark of VadaTech, Inc. Other registered trademarks are the property of their respective owners. AdvancedTCA™ and the AdvancedMC™ logo are trademarks of the PCI Industrial Computers Manufacturers Group. All rights reserved. Specification subject to change without notice.	

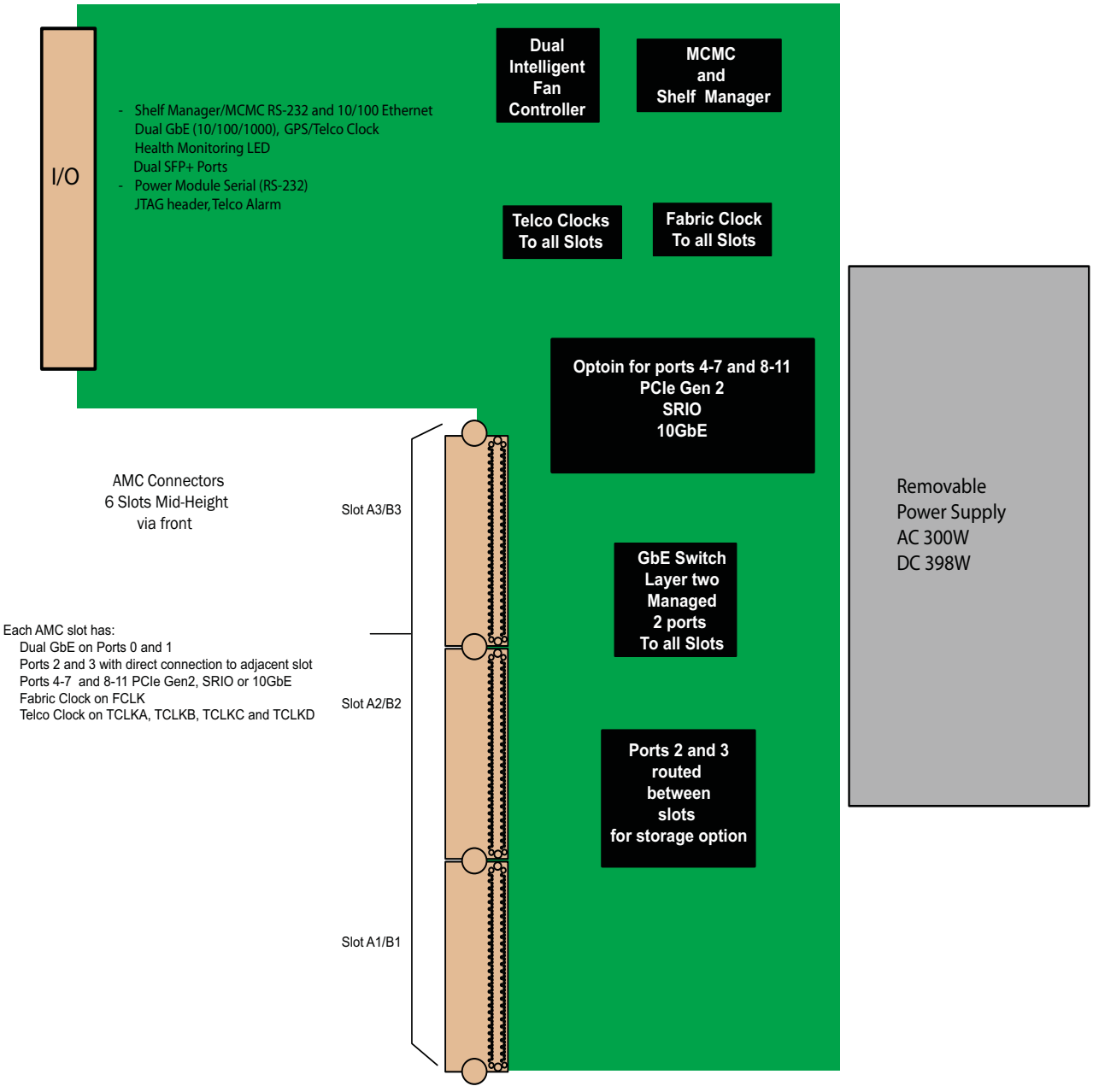


FIGURE 1. VT842 Functional Block Diagram

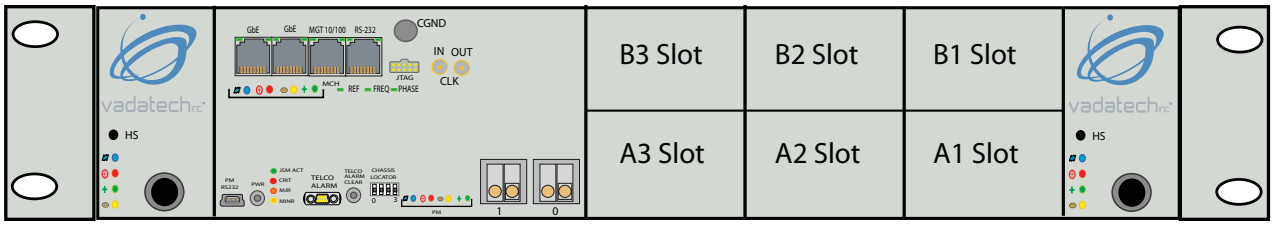
VadaTech can modify this product to meet special customer requirements without NRE (minimum order placement is required).

µTCA 1U Chassis with 6 AMC slots with SFP+

Front

The VT842 front panel provides six AMC slots. The front I/O interface provides out of band 10/100 Ethernet (it interfaces to the Shelf Manager/MCMC directly), Serial interface (RS-232) to the Shelf Manger/MCMC, Dual GbE to the onboard GbE Switch, Dual SFP+ to the 10GbE Fabric, Serial interface (RS-232) to the power module, GPS/Telco clock, as well as provide status indication such as Telco Alarm, Health Monitoring LED, etc.

The front panel also has dual hot swappable Fan Tray.



Rear

The rear of the chassis consists of an A/C socket for the power supply as well as DC input option.

Air flow

The air flow is from right to left. The Air filter is removable from the front.

Key Software Features

- Linux 2.6 embedded OS
- IPMI version 2.0
- Interface to Sensor Data Record repositories, System Event logs, FRU inventory storage devices
- Monitors temperature, voltage and current sensors
- Shelf cooling policy
- Shelf activation and power management
- Alarm controls
- Event notification and flexible alerting policies
- E-Keying
- CLI, SNMP, RMCP+, HTTP and HPI
- IPMI 1.5 compatibility
  - IPMI device global
  - Watchdog timer
  - Session management
  - Event management
  - PEF and alerting
  - Sensor device
  - FRU device access and update
  - SDR device access and update
  - SEL device access and management
  - LAN device configuration
- IPMI 2.0 extension
  - Enhanced encryption
  - Firmware firewall
  - Enhanced authentication

Carrier Manager Functions

- Cooling Management
- LED Controls
- AMC Management
  - Radial IPMB-L
  - Support for 12 AMCs
  - AMC Payload Control
  - Electronic Keying
- Power and Cooling Management

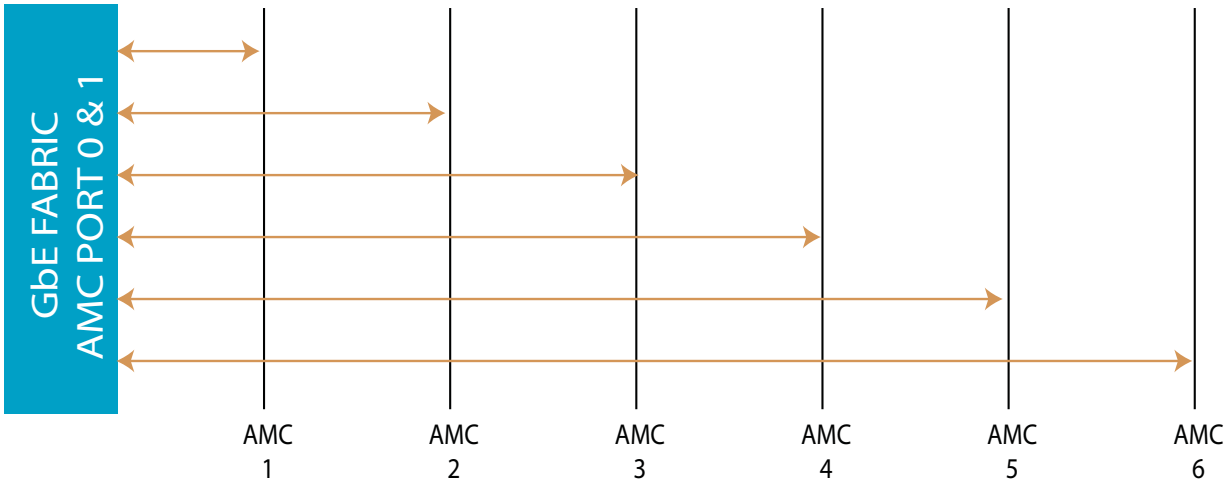
Shelf Manager Functions

- Sensor monitoring and alerting
  - Actively monitors local and remote temperature, voltage and current sensors on the shelf FRUs
  - Access to raw sensor readings
  - Logs all critical events reported by shelf FRUs
  - Events are processed using Platform Event Filtering (PEF)
  - Alerts using SNMP trap and PEF alert policy
  - Capability to reset major/minor alarms with timeout
  - Controls major/minor/critical alarm LEDs

- Shelf manager interface
  - Command Line Interface (CLI)
    - CLI connects to the Shelf Manager and the boards on the shelf
    - IPMI-based library of commands
    - Accessible via telnet, SSH or shelf serial port
    - Commands provide access to information such as the current state of the system, sensor values, events, health, fan speeds, FRU storage, etc.
  - SNMP
    - Supports v1 and v3 of the Simple Network Management Protocol (SNMP)
    - The Shelf Manager can support SNMP queries and send SNMP traps in either v1 or v3
    - Provides custom *Management Information Base (MIB)* tree accessed using SNMP
    - The MIB hierarchy is defined in a text file that describes the shelf and platform objects to be managed and can be used by a remote application such as an SNMP/MIB manager
  - HPI
    - Provides HPI interface to the shelf resources
    - Access to resource tables to enable applications to discover, manage, and monitor the resources in the system:
      - Reset state management
      - Power state management
      - Managed hot swap
      - Alarm management
      - Management instruments associated with entities
      - Event notifications
      - Configuration
      - System and resource event logs

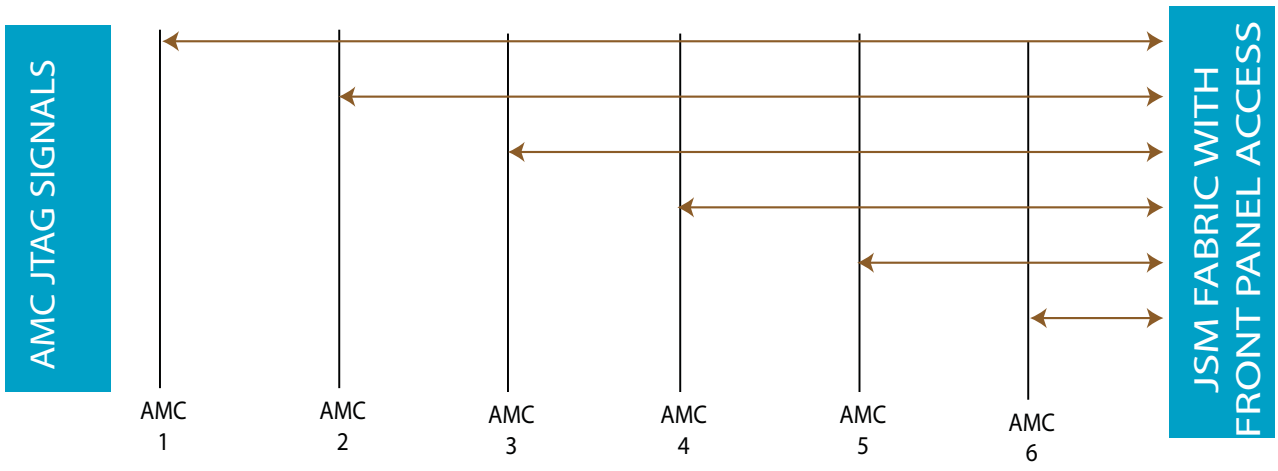
Ports 0 and 1

Port 0 and 1 of each AMC is routed to the on board GbE Fabric.



JTAG Port

Each AMC is routed to the JTAG Switch Module.



Ports 2 and 3

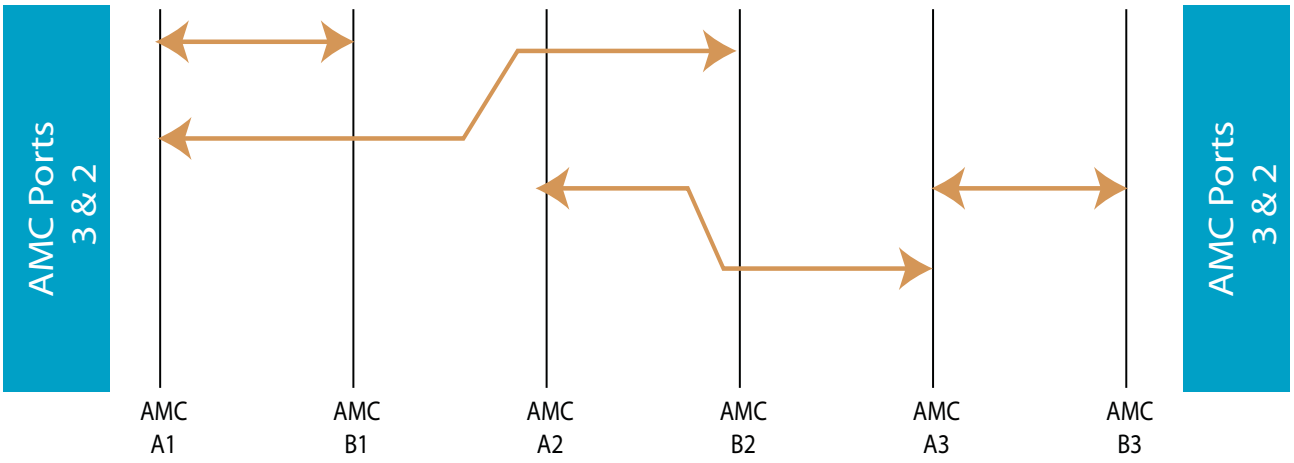
The mid-plane routes ports 2 and 3 among the following slots:

Slot A1 Port 2 --> Slot B1 Port 2

Slot A1 Port 3 --> Slot B2 Port 2

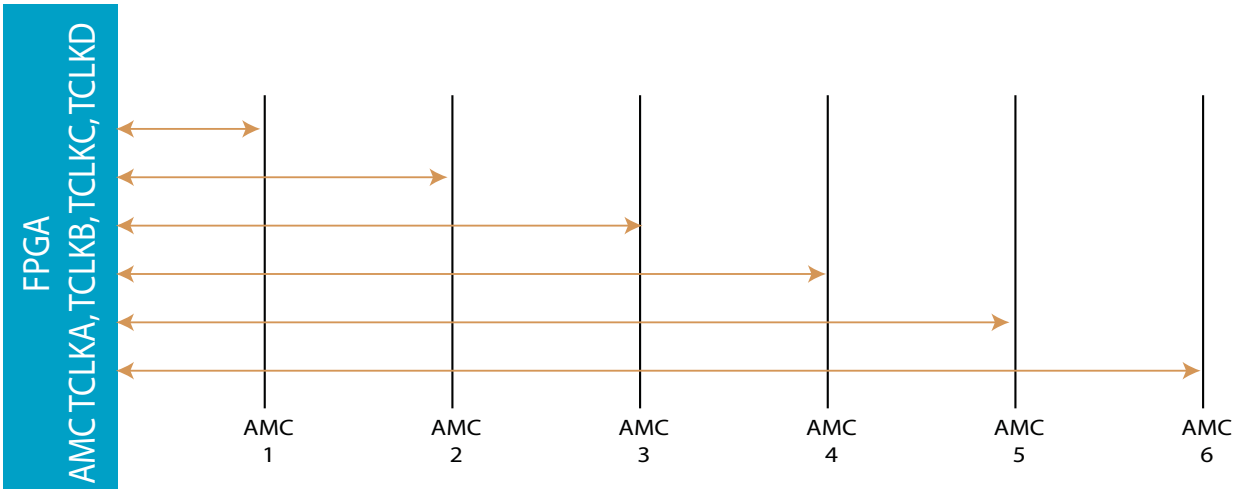
Slot A3 Port 2 --> Slot B3 Port 2

Slot A3 Port 3 ---> Slot A2 Port 2



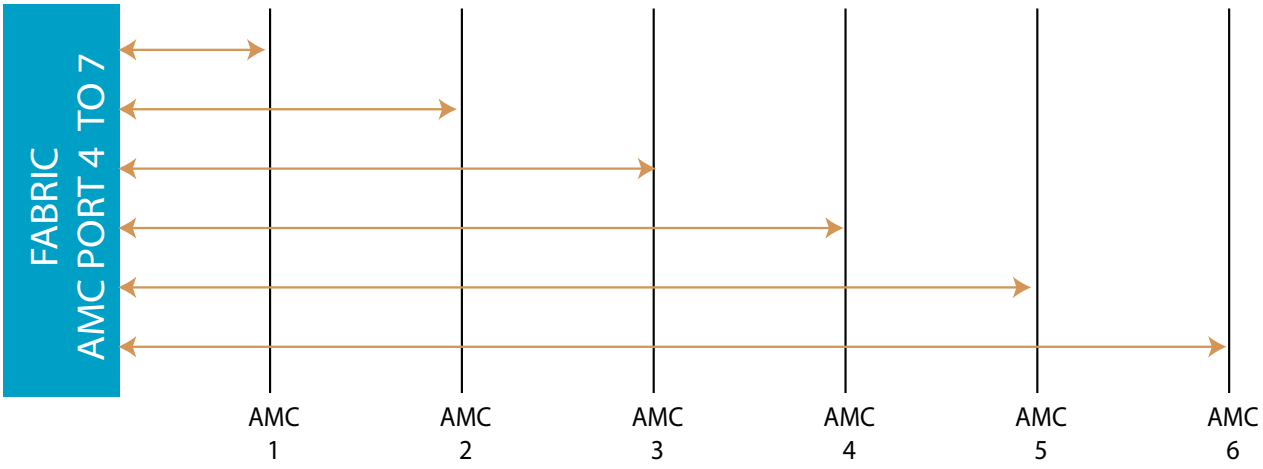
Clock Routing

Fabric clock (FCLK) is routed directly from the clock generator to each AMC. The AMC TCLKA, TCLKB, TCLKC and TCLKD are routed to an on board FPGA for clock routing and configuration.



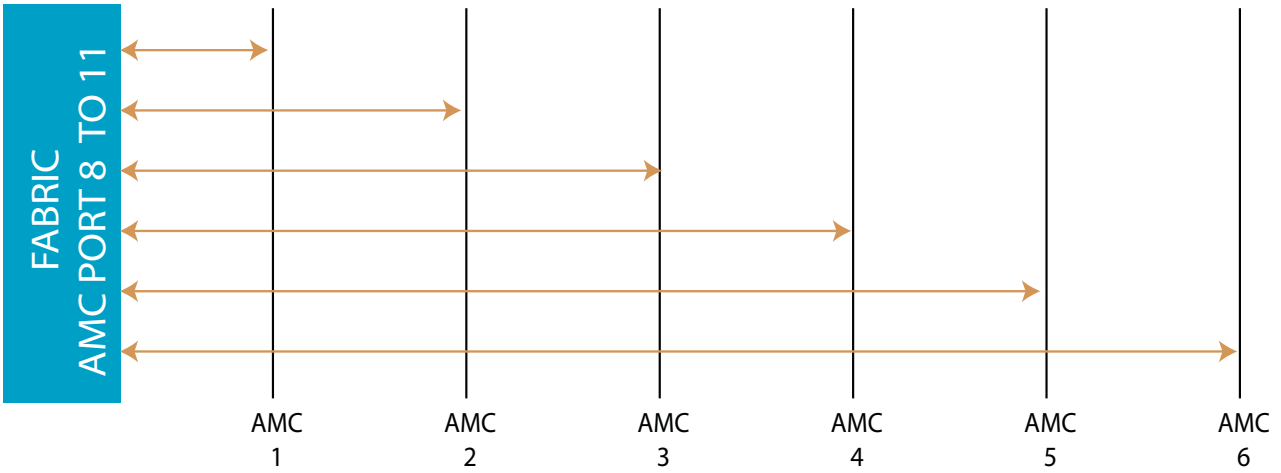
Ports 4 to 7

Ports 4 to 7 are routed to the PCIe Gen2, SRIO or 10GbE switch Fabric.



Ports 8 to 11

Ports 8 to 11 are routed to the PCIe Gen2, SRIO or 10GbE switch Fabric.



NOTE: Since the PCIe Fabric has 12 ports of x4 (48 lanes total) there is option to run all the ports as x8 (on ports 4 to 11) or single dual x4. With the SRIO there are two options, SRIO x4 on all the ports 8-11 or on slots B2 and B3 only.

Each configuration is an ordering option.

Managed Layer Two GbE

Layer Two GbE

The GbE layer two managed switch fabric routes GbE to each of the AMC slots. The GbE fabric has an interface to the on-board Carrier/Shelf manager. It also has a port routed to the front for uplink.

Key features:

- Configuration
  - Ethernet/IEEE 802.3 Packet size (64 bytes to 1522 bytes)
  - Jumbo packets up to 9216 bytes
- L2 Switching
  - Supports up to 8K MAC address
  - Line rate switching for all packet sizes
  - Independent VLAN learning
  - VLAN flooding for broadcast and DLF packets
  - Hardware-based address learning
  - Six CPU-managed learning (CML) modes per port
  - Hardware-and-software-based aging
  - Software insertion/deletion/lookups of the L2 table
  - Same port bridging supported
  - Station movement control
- L2 Multicast
  - 4K VLANs
  - Protocol-based VLANs
  - IEEE 802.1p
  - IEEE 802.1Q
  - Independent VLAN learning (IVL)
  - Ingress filtering for IEEE 802.1Q VLAN security
  - VLAN-based packet filtering
  - MAC-based VLAN
- Source Port Filtering
  - Egress port block masks
  - Trunk group blocking masks
- Storm Control Per-Port:
  - Unknown unicast packet rate control
  - Broadcast packet rate control
  - Multicast packet rate control
- Spanning Tree:
  - IEEE 802.1D spanning tree protocol (single spanning tree per port)
  - IEEE 802.1s for multi spanning trees
  - IEEE 802.1w rapid spanning tree protocol-delete and/or replace per:
    - Port
    - VLAN
    - Port, per VLAN
  - Spanning tree protocol packets detected and sent to the CPU
- Double-Tagging:
  - Unqualified learning/forwarding
  - IEEE 802.1 Q-in-Q

- Mirroring
  - Ingress/egress mirroring support
  - Mirror-to-port receives the unmodified packet for ingress mirroring
  - Mirror-to-port receives the modified packet for egress mirroring
- Content Aware Filter Processing
  - Intelligent Protocol Aware processor with backward-compatible, byte-based classification option
  - Parses up to 128 bytes per packet
  - -512 ACL rules support
  - Multiple matches and actions per packet
  - ACL-based policing
  - Ingress/egress port based filtering
  - MAC destination address remarking
  - Traffic class definition based on the filter
  - Programmable meters allows policing of flows
  - Metering granularity from 64 Kbps to 1Gbps
  - Multiple look-ups per packet
  - Metering support on ingress ports and CPU queues
- QoS Features
  - Four CoS queues per port
  - Per-port, per CoS drop profiles
  - Port level shaping
  - Traffic shaping available on CPU queues
  - Programmable priority to CoS queue mapping
  - Provides two levels of drop precedence per queue
  - Strict Priority (SP), Weighted Round Robin (WRR), and Deficit round Robin (DRR) mechanisms for shaped queue selection
- DSCP
  - DSCP-based prioritization
  - Back pressure metering
  - DSCP to IEEE 802.1p mapping
- Port Security
  - Per port blocking
  - Supports IEEE 802.1x
  - MAC address blocking
- DoS Prevention
  - Denial of Service detection/prevention
- Management Information Base
  - SMON MIB, IETF RFC 2613
  - RMON statistics group, IETF RFC 2819
  - SNMP interface group, IETF RFC 1213, 2836
  - Ethernet-like MIB, IETF RFC 1643
  - Ethernet MIB, IEEE 802.3u
  - Bridge MIB, IETF RFC 1493

Layer Three GbE

Please Contact VadaTech Sales for features and options.

Telcom, GPS and Fabric Clocks

The µTCA specification defines a set of clocks for Telcom and non-Telcom applications. The VadaTech VT842 has the most sophisticated clocking distribution in the market to meet the most stringent requirements such as wireless infrastructure, high speed A/D, etc. The VT842 has three types of clocks defined:

- Telcom clock
- GPS clock
- Fabric clock

The VT842 has two SMA clock connectors on the front panel. One is used as an external reference clock and the second one is an output for expansion. This provides the most flexibility to the overall system architecture.

Telcom Clock T1/E1/SDH Stratum 3 Redundant System Clock Synchronizer

The SDH/PDH System Synchronizer contains a DPLL which provides timing and synchronization for SDH and T1/E1. The module generates SBI, ST-Bus and other TDM clock and framing signals that are phase locked to any of the AMC clocks, BITS via the front panel SMA connector or to the system master-clock. The reference clock is a Stratum-3 TCXO. The module monitors its references for frequency accuracy and stability and by maintaining tight phase alignment between the master-clock and slave-clock outputs even in the presence of high network jitter.

Key features:

- Synchronizes to clock-and-sync pair to maintain minimal phase skew between the master-clock and the redundant slave-clock
- ITU G.813 option 1, G.823 for 2048 kbit/s and G.824 for 1533kbit/s interfaces
- Telcordia GR-1244-Core stratum 3/4/4E
- ANSI T1.403 and ETSI ETS 300 011 for ISDN primary rate interface
- Accepts three input references and synchronized to any combination of 2 KHz, 8 KHz, 1.544 MHz, 2.048 MHz, 8.192 MHz, 16.384 MHz or 19.44 MHz inputs
- Provides a range of available clock outputs to the backplane and front panel connector: 1.544 MHz (DS1), 2.048 MHz (E1), 3.088 MHz, 16.384 MHz, and 19.44 MHz (SDH), and either 4.096 MHz and 8.192 MHz or 32.768 MHz and 65.536 MHz, and a choice of 6.312 MHz (DS2), 8.448 MHz (E2), 44.736 MHz (DS3) or 34.368 MHz (E3)
- Provides 5 styles of 8 KHz framing pulses and a 2 KHz multi-frame pulse
- Holdover frequency accuracy of $1x10^{-8}$
- Selectable loop filter 1.8 Hz, 3.6 Hz or 922 Hz
- Less than 24 psrms intrinsic jitter on the 19.44 MHz output clock, compliant with GR-253-CORE OC-3 and G.813 STM-1 specifications
- Less than 0.6 nspp intrinsic jitter on all output clocks and frame pulses
- Manual or Automatic hitless reference switching between any combination of valid input reference frequencies
- Provides Lock, Holdover and selectable Out of Range indication
- Front panel Reference Good and PLL Locked LED indicators

GPS Clock

The VT842 can take GPS 1 PPS in and create a 30.72MHz clock (Frequencies from 8MHz to 52MHz are available, default is 30.72MHz) which is phased aligned. The clock complies with Telcordia's GR-1244-Core for Stratum 3 applications which ensures precise network timing and synchronization. It can be utilized in wireless applications such as Worldwide Interoperability for Microwave Access (WiMAX). The module can output any of the available clocks via the front panel clock output at the customer's request.

If the GPS 1 PPS is lost the module will automatically enter a holdover mode to maintain timing.

Key features:

- 30.72MHz* frequency / phase-synchronized based on the GPS 1 PPS
- On board Stratum-3 TCVCXO
- Holdover in case of loss of signal from GPS
- Provides a buffered 1 PPS output (including during holdover)
- Front panel Reference Good, Frequency Locked, and Phase Locked LED indicators

*The 30.72MHz is the default configuration for WiMAX applications. Frequencies from 8MHz to 52MHz are available.

Fabric Clock

The VT842 has the capability to provide Fabric clocks. The Fabric clocks are HCSL and run at 100MHz with a very low Jitter to meet the PCIe Gen 2 specification.

Key features:

- 0.7V Current mode differential HCSL output
- Output frequency of 100MHZ
- RMS period Jitter 3 ps (maximum)
- Cycle-to-cycle jitter: 35 ps (maximum)
- Spread Spectrum capable for EMI reduction

Fabrics on Ports 4-7 and 8-11

The VT842 supports the following fabrics:

- PCIe Gen 2
- 10 GbE layer three managed (option for unmanaged)
- SRIO

PCIe Gen 2

The PCIe fabric is Gen 2 and is non-blocking on all the ports. PCIe Gen 2 allows 5 Gbps on each link, which is twice the speed of Gen 1 at 2.5 Gbps.

Each of the AMCs receives 8 lanes of PCIe which each AMC can negotiate down to PCIe Gen 1 independent of other ports. This allows modules in the system to be mix of Gen 1 and Gen 2 PCIe.

Key features:

- 48 Lanes with 12 independent ports
- Fully non-blocking
- Dynamic speed negotiation (2.5 or 5.0 Gbps)
- Dynamic link width negotiation
- Non-Transparent bridging capability
- Enable Dual-Host, Dual-Fabric, and Host-Fail-over applications
- 480 GT/s aggregated bandwidth
- Cut-Thru packet latency of less then 140ns

SRIO Fabric

The SRIO switch Fabric supports revision 1.3 of the RapidIO Interconnect Specification. It has a single SRIO 40 lane chip or dual 40 lanes on board. With the single SRIO chip all of the AMC slots have an x4 connection on ports 4-7 in addition with two AMC slots (B2 and B3) having an x4 connection on ports 8-11. With the Dual 40 Lane SRIO module all the AMC slots have dual x4 connection (ports 4-7 and 8-11).

Key Features:

- Port frequency configuration from 1.25, 2.5 and 3.125 Gbits/s
- 100Gbps of switching bandwidth per switch Fabric
- 64,000 Endpoints through hierarchical lookup
- Independent unicast and multicast routing mechanism
- Supports up to 40 simultaneous multicast masks per fabric chip
- Error management extensions
- All configurations are via I2C bus
- Packet Trace function: It allows filtering out packets that contain a match

10 GbE Layer 3 Managed switch

The 10GbE switch fabric is layer two/three managed and each of the AMC modules has a 10GbE interface to the Fabric. Further there is two SFP+ connector in the front which is used for expansion. This switch has the richest set of features in the market by running carrier grade management software under Linux.

Key features:

- Spanning Tree Protocol (STP)
- Rapid Spanning Tree Protocol (RSTP)
- Multiple Spanning Tree Protocol (MSTP)
- Virtual LANs (VLANs)
- Generic Attribute Registration Protocol (GARP)
- Generic Multicast Registration Protocol (GMRP)
- Generic VLAN Registration Protocol (GVRP)
- Port Authentication
- Internet Group Management Protocol (IGMP) (Version 1, 2, and 3) Snooping/Proxy
- Multicast Listener Discovery (Version 1, 2) Snooping/Proxy
- Provider Bridging IEEE802.1 ad/D6.0
- Multiple Registration Protocol (MRP) IEEE802.1ak/D4.0
- Multiple multicast Registration Protocol (MMRP) IEEE802.1ak/D4.0
- Multiple VLAN Registration Protocol (MVRP) IEEE802.1ak/D4
- Link Layer Discovery Protocol IEEE802.1AB 2005
- Ethernet OAM IEEE 802.3ah -2004 clause 57
- Connectivity Fault Management IEEE802.1ag -d6.0
- Link Aggregation - Static; IEEE802.3ad (2002); IEEE8023 LAG-MIB
- Open Shortest Path First (OSPFv2/OSPFv3)
- Routing Information Protocol (RIP/RIPng)
- Border Gateway Protocol (BGP4/BGP4+)
- Intermediate System-to-Intermediate System (IS-IS)
- Layer 2 VPNs

ORDERING OPTIONS

VT842 - ABC - DEF- GHJ

A = Management Software

1 = MCMC
2 = MCMC and Shelf Manager

B = JSM

0 = None
1 = Included

C = Fabric on Ports 4-7 and 8-11

0 = None
1 = 10GbE Full Managed Layer 2/3
2 = 10GbE Light Managed
3 = PCIe Gen2 on ports 4-7 and 10GbE on ports 8-11

D = SFP+ Transceivers Port 0

0 = None
1= 10GBASE-SR
2 = Reserved
3 = 10GBASE-LRM
4 = 10GBASE-LR

E = SFP+ Transceivers Port 1

0 = None
1= 10GBASE-SR
2 = Reserved
3 = 10GBASE-LRM
4 = 10GBASE-LR

F = Telcom/GPS Clock

0 = None
1 = Clock Distribution only
2 = Telcom TCXO**
3 = GPS TCVCXO** 30.72MHz†
4 = GPS TCVCXO** 10.00MHz†
5 = Reserved

G = Power Supply

0 = AC Universal
1 = DC -36 to -75V

H = Operating Temp

1 = Commercial
2 = Industrial

J = Conformal Coating

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic

**The Crystal Oscillator is Stratum-3; for lower cost solutions contact VadaTech Sales.

†Frequencies from 8MHz to 52MHz are available.

Back view of the VT842 with the AC power supply

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