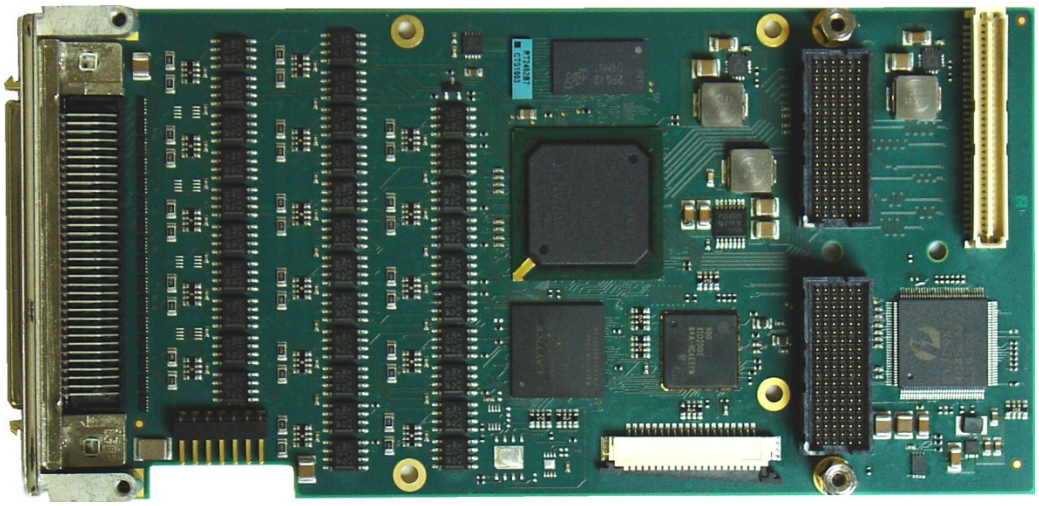
TXMC633 Reconfigurable FPGA with 64 TTL I/O / 32 Diff. I/O



TXMC633-23R

Application Information

The TXMC633 is a standard single-width Switched Mezzanine Card (XMC) compatible module providing a user configurable XC6SLX45T-2 or XC6SLX100T-2 Spartan-6 FPGA.

The TXMC633-x0R has 64 ESD-protected TTL lines; the TXMC633-x1R provides 32 differential I/O lines using EIA 422 / EIA 485 compatible, ESD-protected line transceivers. The TXMC633-x2R provides 32 TTL and 16 differential I/Os. The TXMC633-x3R provides 32 differential I/O lines using Multipoint-LVDS Transceiver. The TXMC633-x4R provides 32 TTL and 16 differential I/O Multipoint-LVDS Transceiver.

For customer specific I/O extension or inter-board communication, the TXMC633-xx provides 64 FPGA I/Os on P14 and 3 FPGA Multi-Gigabit-Transceiver on P16. P14 I/O lines could be configured as 64 single ended LVCMOS33 or as 32 differential LVDS33 interface.

All I/O lines are individually programmable as input or output. Setting as input sets the I/O line to tri-state and could be used with on-board pull-up also as tri-stated output. Each TTL I/O line has a pull-resistor. The pull-voltage level is programmable to be either +3.3V, +5V and additionally GND. The differential RS485 I/O lines are terminated by 120Ω resistors and the differential MLVDS I/O lines are terminated by 100Ω resistors.

The User FPGA is connected to a 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses a hardwired internal Memory Controller Block of the Spartan-6.

The User FPGA is configured by a platform SPI flash or via PCIe download. The flash device is in-system programmable. An in-circuit debugging option is available via a JTAG header for read back and real-time debugging of the FPGA design (using Xilinx “ChipScope”).

The direct configuration via PCIe of the User FPGA is realized by the Configuration FPGA. Configuration data is programmed via 32 bit transfer register to the User FPGA (Spartan6). Data source are XILINX ISE binary files (.bit file or .bin file) which are generated by XILINX ISE Design Software. These binary files consist of header, preamble and configuration data. Only configuration data must be transferred. See also the XILINX User Guide (ug380) “Spartan6 FPGA Configuration” for more information about configuration details and configuration data file formats.

User applications for the TXMC633 with XC6SLX45T-2 FPGA can be developed using the design software ISE Project Navigator (ISE) and Embedded Development Kit (EDK). IDE versions are 14.7. Licenses for both design tools are required.

TEWS offers a well-documented basic FPGA Example Application design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers the main functionalities of the TXMC633. It implements local Bus interface to local Bridge device, register mapping, DDR3 memory access and basic I/O. It comes as a Xilinx ISE project with source code and as a ready-to-download bit stream.

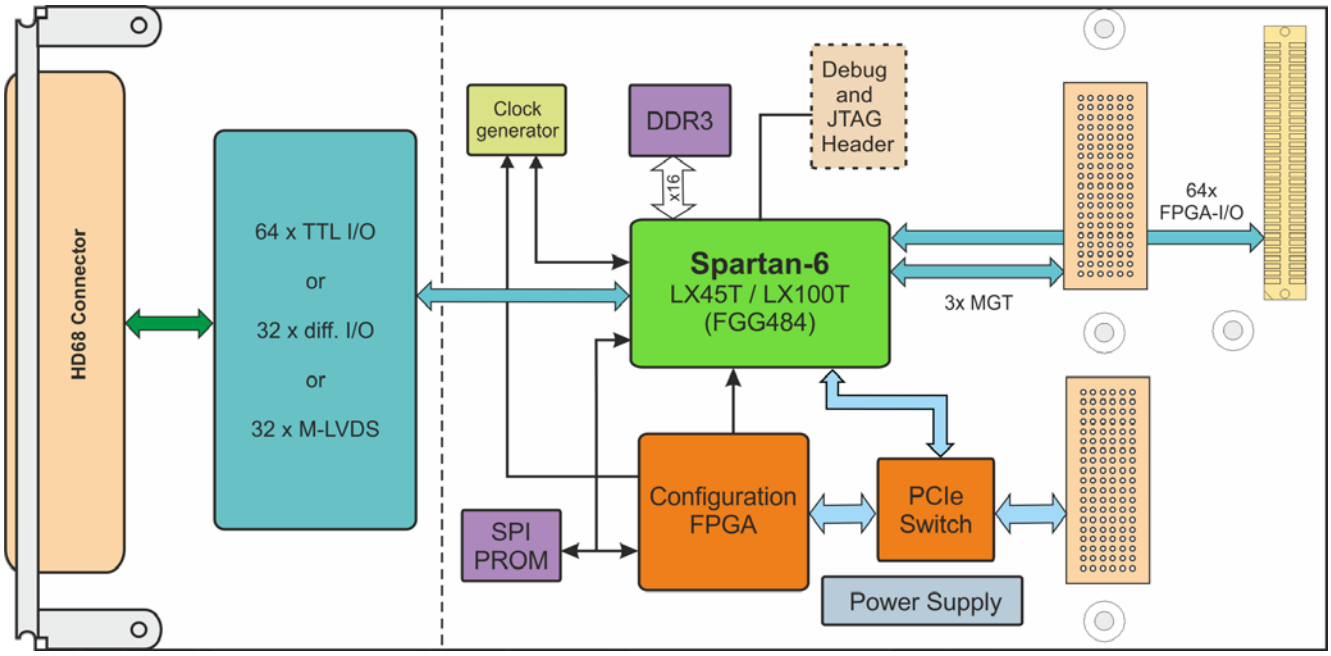
Issue 1.0.1
2015-04-09

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Technical Information

- Form Factor: Standard single-width XMC module conforming to ANSI/VITA 42.0-2008
  - Board size: 149 mm x 74 mm
- PCI Express (Base Specification 1.1) compliant interface conforming to ANSI/VITA 42.3-2006
- IPMI resource: FRU hardware definition information stored in on-board EEPROM
- TXMC633-1xR: Xilinx XC6SLX45T-2 Spartan6 FPGA configured by serial Flash
  TXMC633-2xR: Xilinx XC6SLX100T-2 Spartan6 FPGA configured by serial Flash
- FPGA clock options:
  - Local clock generator as source for the FPGA internal PLL

  1 DDR3 SDRAM bank, 64M x 16 (128 MB)
- 32 Mbit SPI-EEPROM for User Data and FPGA configuration
- Front I/O lines
  64 TTL I/O, or 32 differential I/O or 32 TTL I/O and 16 differential I/O
  - TTL signaling voltage (maximum current: +/- 32mA), EIA-422/-485 signaling level or M-LVDS Standard (TIA/EIA-899)
  - direction individually programmable
- Back I/O lines
  64 FPGA I/Os on P14 and 3 FPGA Multi-Gigabit-Transceiver on P16
  - P14 with 64 single ended LVCMOS33 or 32 differential LVDS33 depends on Spartan6 Configuration
- I/O access:
  - 64 I/O lines on HD68 front connector
  - 64 I/O lines on P14 Mezzanine connector
  - 3 MGT RxTx lines on P16 Mezzanine connector
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G_B 20°C): 320000 h



TXMC633 Block Diagram

Issue 1.0.1
2015-04-09

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Order Information

RoHS Compliant

TXMC633-10R	Spartan-6 FPGA XC6SLX45T-2,128 MB DDR3	64 TTL I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-11R	Spartan-6 FPGA XC6SLX45T-2,128 MB DDR3	32 Diff. I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-12R	Spartan-6 FPGA XC6SLX45T-2,128 MB DDR3	32 TTL I/O and 16 Diff. I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-13R	Spartan-6 FPGA XC6SLX45T-2,128 MB DDR3	32 M-LVDS I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-14R	Spartan-6 FPGA XC6SLX45T-2,128 MB DDR3	32 TTL I/O and 16 M-LVDS I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-20R	Spartan-6 FPGA XC6SLX100T-2,128 MB DDR3	64 TTL I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-21R	Spartan-6 FPGA XC6SLX100T-2,128 MB DDR3	32 Diff. I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-22R	Spartan-6 FPGA XC6SLX100T-2,128 MB DDR3	32 TTL I/O and 16 Diff. I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-23R	Spartan-6 FPGA XC6SLX100T-2,128 MB DDR3	32 M-LVDS I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16
TXMC633-24R	Spartan-6 FPGA XC6SLX100T-2,128 MB DDR3	32 TTL I/O and 16 M-LVDS I/O on HD68 64 direct FPGA I/O on P14, 3 MGTs on P16

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TXMC633-DOC User Manual

Software

For Software Support please contact TEWS.

Related Products

TA304 Cable Kit for modules with HD68 SCSI-3 type connector
TPIM003 PIM I/O Module with HD68 SCSI-3 type connector and special pin assignment

TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com