

# AMC FPGA Carrier with FMC Interface

## AMC515



### KEY FEATURES

- AMC FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-57
- AMC Ports 4-11 are routed to FPGA (protocols such as PCIe, SRIO, XAUI, etc. are FPGA programmable)
- Xilinx Virtex-7 XC7V2000T in 1925 package
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD
- On board PLL for buffering/multiplying and jitter cleaner
- Option for 2GB of DDR-III memory to FPGA
- On board Freescale QorIQ PPC2040 with 2 GB DDR-III
- Serial Over LAN (SOL) with hardware RNG
- RoHS compliant

The AMC515 is an AMC FPGA Carrier with an FMC (VITA 57) interface. The AMC515 is compliant to the AMC.1, AMC.2 and/or AMC.4 specification. The unit has an on-board, re-configurable FPGA which interfaces directly to the AMC Ports 4-11, FCLKA, TCLKA, TCLKB, TCLKC, and TCLKD. The FPGA has an interface to a bank of DDR-III memory (64-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The AMC515 have ports 12-15 and 17-20 routed as LVDS.

The AMC515 has a single FMC connector per VITA-57. This allows having a single Carrier with multiple-different FMC modules in the system.

The on board PPC runs at 1.2GHz with 2GB of DDR-III, 8Mbytes of boot flash and up to 32GBytes of user Flash. The PPC has an x1 PCIe interface to the FPGA in addition to it's local bus. The PPC has dual GbE routed to ports 0 and 1 of the AMC as well as a GbE to the FPGA. The AMC515 has Serial Over LAN per IPMI specification. It has hardware RNG (Random Number Generator) for secure session.

VadaTech can modify this product to meet special customer requirements without NRE (minimum order placement is required).

**AdvancedMC™**

# AMC FPGA Carrier with FMC Interface

## SPECIFICATIONS

Architecture		
Physical	Dimensions	Single-width, Full-Height
		Width: 2.89 in. (73.5 mm)
		Depth: 7.11 in. (180.6 mm)
Type	AMC FPGA Carrier	Xilinx FGPA Virtex-7 Device XC7V2000T in 1925 Package
		PLL multiplier/divider with jitter cleaner
		Single FMC slot
		Single bank of DDR-III
Standards		
AMC	Type	AMC.1, AMC.2, and AMC.4 (FPGA programmable)
Module Management	IPMI	IPMI Version 2.0
PCIe	Lanes	x4 or x8
SRIO	Lanes	Dual x4
XAUI	Lanes	Dual port XAUI
Aurora	Lanes	Dual x4
Ethernet	GbE	Dual 1000-BaseBX from PPC
Configuration		
Power	AMC515	Carrier is 40W max without the Mezzanine
Environmental	Temperature	Operating Temperature: 0° to 65° C (Air flow requirement is to be greater than 400 LFM)
		Storage Temperature: -40° to +90° C
	Vibration	1G, 5-500Hz each axis
	Shock	30Gs each axis
	Relative Humidity	5 to 95 percent, non-condensing
Front Panel	Interface Connectors	Front panel FMC
	LEDs	IPMI Management Control
		8 user defined LED
	Mechanical	Hot Swap Ejector Handle
Software Support	Operating Systems	Linux, Windows, Solaris and VxWorks
Other		
MTBF	MIL Handbook 217-F > TBD.	
Certifications	Designed to meet FCC, CE and UL certifications where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Compliance	RoHS and NEBS	
Warranty	Two (2) years.	
Trademarks and Logos	The VadaTech logo is a registered trademark of VadaTech, Inc. Other registered trademarks are the property of their respective owners. AdvancedMC™ and the AdvancedTCA™ logo are trademarks of the PCI Industrial Computers Manufacturers Group. All rights reserved. Specification subject to change without notice.	

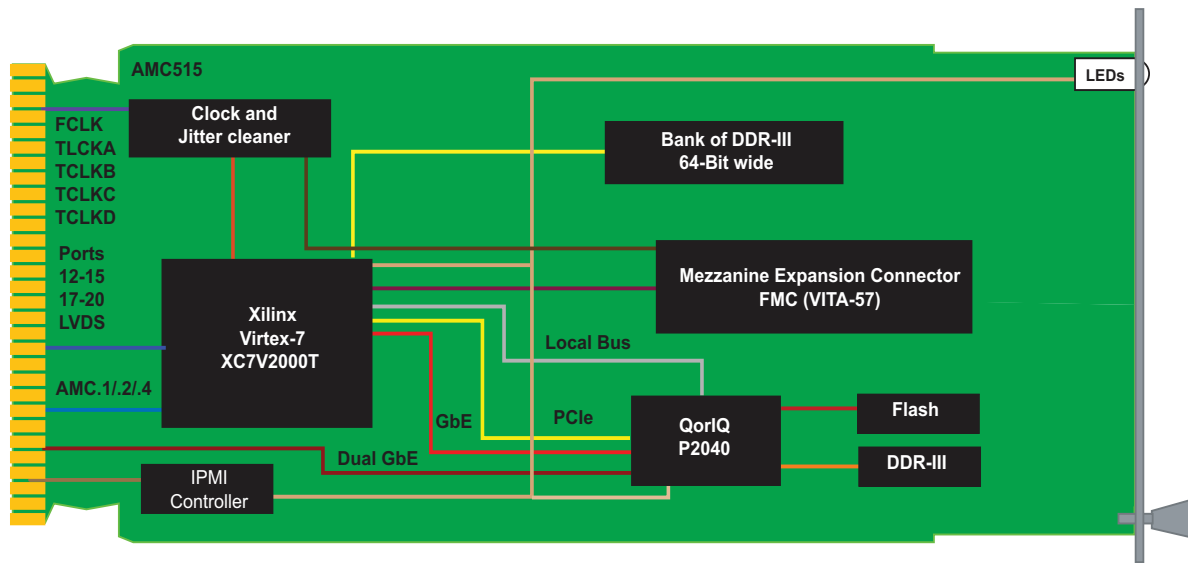
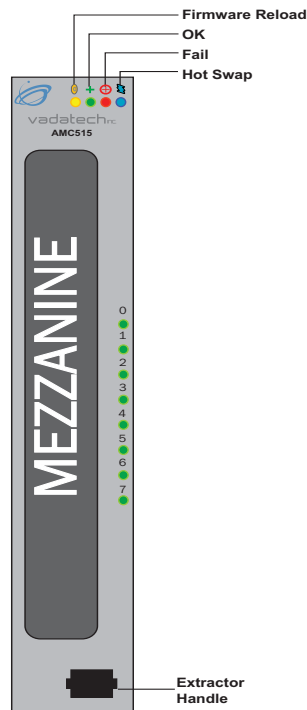


FIGURE 1. AMC515 Functional Block Diagram

FIGURE 2. AMC515 Front Panel



## ORDERING OPTIONS

### AMC515 - ABC - DE0 - OHJ

#### A = FPGA DDR-III Memory

- 0 = None
- 1 = 1GB
- 2 = 2GB

#### B = FPGA SPEED

- 1 = Low
- 2 = High

#### C = Front Panel

- 1 = Reserved
- 2 = Mid-Height
- 3 = Full-Height

#### D = FPGA PCIe option

- 0 = No PCIe (ports 4-11)
- 1 = PCIe on ports 4-7
- 2 = PCIe on ports 8-11
- 3 = PCIe on ports 4-11

#### E = PPC Nand Flash

- 0 = 16GB
- 1 = 32GB

#### H = Operating Temp

- 0 = Commercial
- 1 = Industrial

#### J = Conformal Coating

- 0 = None
- 1 = Humiseal 1A33 Polyurethane
- 2 = Humiseal 1B31 Acrylic

