Low Cost AMC FPGA Carrier with FMC Interface

# AMC518

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## KEY FEATURES

- AMC FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-57
- Xilinx Spartan-6 FPGA in FG-484 package
- Option for up to 256MB of FPGA DDR-III memory
- AMC Port 4 and FMC DP0 are routed to FPGA (protocols such as GbE, PCIe, SRIO, etc. are FPGA programmable)
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed
- On board PLL for buffering/multiplying and jitter cleaner
- Flexible programmable clock from 5KHz to 500MHz via I2C Bus
- RoHS compliant

The AMC518 is an AMC FPGA Carrier with an FMC (VITA 57) interface. The AMC518 is compliant to the AMC.1, AMC.2 and/or AMC.4 specification. The unit has an on-board, re-configurable FPGA which interfaces directly to AMC Port 4, FCLKA, TCLKA, TCLKB, TCLKC, and TCLKD. The FPGA interfaces to a DDR-III single-chip memory (16-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The AMC518 has a single FMC connector per VITA-57. This allows having a single carrier with multiple different FMC modules in the system.

A programmable Clock Generator can synthesize frequencies from 5KHz to 500MHz from its 1.3GHz VCO. Three clocks are routed from the Clock Generator to the FPGA.

VadaTech can modify this product to meet special customer requirements without NRE (minimum order placement is required).

AdvancedMC™

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## SPECIFICATIONS

| | | |
|---|---|---|
| **Architecture** | | |
| **Physical** | **Dimensions** | Single-width, Mid-Height (option for Full-Height) |
| | | Width: 2.89 in. (73.5 mm) |
| | | Depth: 7.11 in. (180.6 mm) |
| **Type** | **AMC FPGA Carrier** | Xilinx FGPA Spartan-6 Devices |
| | | PLL multiplier/divider with jitter cleaner |
| | | Single FMC slot |
| | | Single bank of DDR-III (16-bit) |
| **Standards** | | |
| **AMC** | **Type** | AMC.1, AMC.2, and AMC.4 (FPGA programmable) |
| **Module Management** | **IPMI** | IPMI Version 2.0 |
| **PCIe** | **Lanes** | x1 via FPGA |
| **SRIO** | **Lanes** | x1 via FPGA |
| **Configuration** | | |
| **Power** | **AMC518** | Carrier is 6W without the Mezzanine (FPGA dependent) |
| **Environmental** | **Temperature** | Operating Temperature: 0° to 65° C (Air flow requirement is to be greater than 400 LFM) |
| | | Storage Temperature: -40° to +90° C |
| | **Vibration** | 1G, 5-500Hz each axis |
| | **Shock** | 30Gs each axis |
| | **Relative Humidity** | 5 to 95 percent, non-condensing |
| **Front Panel** | **Interface Connectors** | Front panel FMC |
| | **LEDs** | IPMI Management Control |
| | | 8 user defined LED |
| | **Mechanical** | Hot Swap Ejector Handle |
| **Software Support** | **Operating Systems** | Linux, Windows, Solaris and VxWorks |
| **Other** | | |
| **MTBF** | MIL Handbook 217-F > TBD. | |
| **Certifications** | Designed to meet FCC, CE and UL certifications where applicable | |
| **Standards** | VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards | |
| **Compliance** | RoHS and NEBS | |
| **Warranty** | Two (2) years. | |
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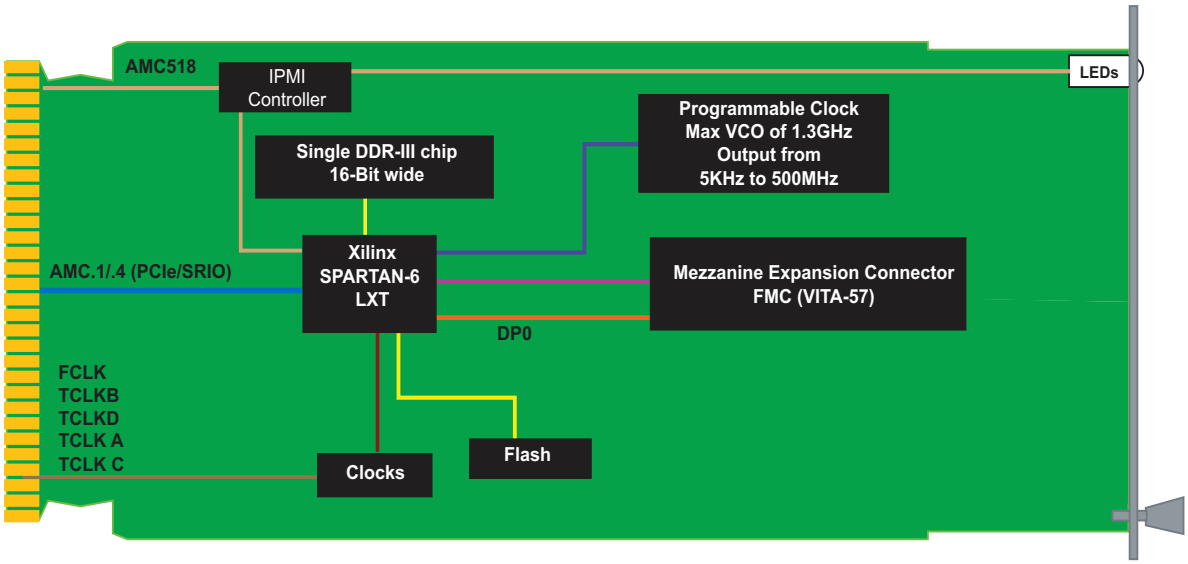
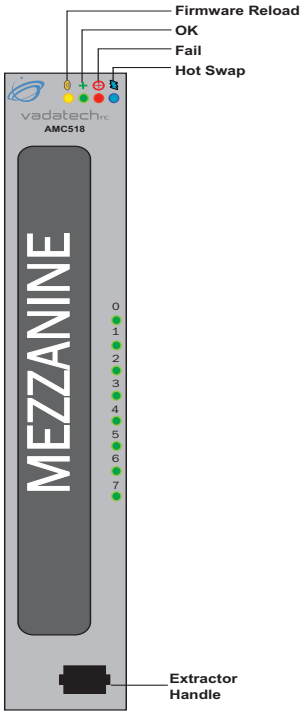



FIGURE 1. AMC518 Functional Block Diagram

FIGURE 2. AMC518 Front Panel



## ORDERING OPTIONS

**AMC518 - A0C - DE0 - 0HJ**

**A = DDR-III Memory**

0 = None
1 = 256MB (single chip)

**D = FPGA***

2 = XC6SLX25T
3 = XC6SLX45T
4 = XC6SLX75T
3 = XC6SLX100T
4 = XC6SLX150T

**E = FPGA SPEED**

2 = Low
3 = High

**H = Operating Temp**

0 = Commercial
1 = Industrial

**C = Front Panel**

1 = Reserved
2 = Mid-Height
3 = Full-Height

**J = Conformal Coating**

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic

* The various FPGA density options have variable numbers of pins available for FMC I/O. Please contact VadaTech for more details.

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