

AMC Stratix V FPGA, 100G -AMC534

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KEY FEATURES

- Altera Stratix V GT FPGA in FFG-1517 package
- Dual zQSFP+ ports to the front panel
- Front panel Port 0 at 100G, Port 1 at up to 40G
- AMC Ports 4-7 and 8-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (protocols such as PCIe, SRIO, XAUI, XLAUI, etc. are FPGA programmable)
- On-board Freescale QorIQ PPC2040 with DDR3
- FPGA can load via Flash or via the P2040
- FPGA Flash can be programmed via the JTAG or the P2040
- Serial over LAN (SOL) with hardware RNG
- IPMI 2.0 compliant

AdvancedMC™

Benefits of Choosing VadaTech

- 100G performance through one port and up to 40G performance in the 2nd port via the front panel
- Distributed processing with local P2040 processor provides more reliability, performance and eliminates a potential single-point-of-failure in the system
- Design utilizes proven VadaTech subcomponents and engineering techniques
- Electrical, mechanical, software, and system-level expertise in house
- Full ecosystem of front and rear boards, enclosures, specialty modules, and test/dev products from one source
- AS9100 and ISO9001 certified company

The AMC534 is an FPGA with dual zQSFP+ connectors offering 100G performance (Port 0 at 100G, Port 1 up to 40G) via the front panel. The module is compliant to the AMC.1, AMC.2, and/or AMC.4 specification. It has an on-board, reconfigurable FPGA which interfaces directly to the AMC FCLKA and TCLK A-D. The FPGA has interfaces to four DDR3 memory channels (32-bit wide each) with 1 GBytes per channel and a 4 GBytes total size. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The on-board quad-core P2040 can run at 1.2GHz with 2 GBytes of DDR3, 128 Mbytes of Boot Flash, and a 32 GByte SD Card. The PPC has an x4 PCIe interface to the FPGA in addition to its local bus. The PPC has its dual GbE routed to ports 0 and 1 of the AMC.

The AMC534 has Serial over LAN per the IPMI specification and a hardware RNG (Random Number Generator) for secure session.

VadaTech can modify this product to meet special customer requirements. Contact us to discuss your application.

REFERENCE DESIGN

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is geared to prove out the hardware for engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application.

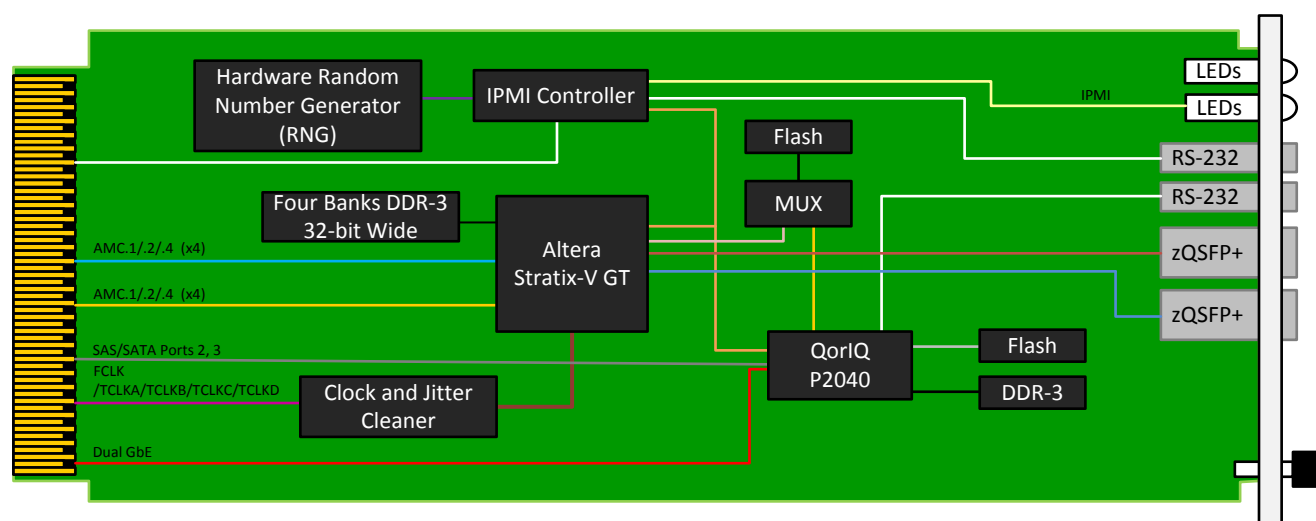
FRONT PANEL zQSFP+ PORTS

The front panel zQSFP+ Ethernet ports provide support for 10GbE/40GbE/100GbE via removable QSFP+ or zQSFP+ modules. There are not any status LEDs directly associated with these ports. Port 0 routes to GTB transceiver ports on the FPGA and is limited to an operating range of 20 Gbps to 28.05 Gbps per lane (100GbE utilizing four lanes). Port 1 routes to GXB transceiver ports on the FPGA and is limited to an operating range of 600 Mbps to 12.5 Gbps per lane (10GbE/40GbE utilizing four lanes). The ports are protocol agnostic and can be used for any SERDES protocol that is compatible with both the zQSFP+ module and the FPGA's transceivers.

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of ATCA and μ TCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTM), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

BLOCK DIAGRAM



FRONT PANEL



SPECIFICATIONS

Architecture		
Physical	Dimensions	Width: 2.89" (73.5 mm)
		Depth 7.11" (180.6 mm)
Type	AMC FPGA Carrier	Altera FPGA Stratix-V GT Device
		On-board CPU
		Four banks of DDR3 (32 bits each)
Standards		
AMC	Type	AMC.1, AMC.2, and AMC.4 (FPGA programmable) and AMC.3
Module Management	IPMI	IPMI version 2.0
PCIe	Lanes	Dual x4 via FPGA to AMC
SRIO	Lanes	Dual x4 via FPGA to AMC
Ethernet	10GbE and GbE	Dual 10GbE via FPGA and dual 1000 BaseBX from PPC
Configuration		
Power	AMC534	Carrier is ~40W (without mezzanine) application specific
Environmental	Temperature	Operating Temperature: -5° to 55°C (air flow > 400LFM) industrial and military versions also available (See environmental spec sheet)
		Storage Temperature: -40° to +90°C
	Vibration	Operating 9.8 m/s², 1G, 5 to 500Hz on each axis
	Shock	Operating 30G on each axis
	Relative Humidity	5 to 95 per cent, non-condensing
Front Panel	Interface Connectors	Dual zQSFP+, CPU RS-232
	LEDs	IPMI management control
		Activity / Link user LEDs
	Mechanical	Hot swap ejector handle
Software Support	Operating System	Linux, VxWorks
Other		
MTBF	MIL Handbook 217-F@TBD Hrs	
Certifications	Designed to meet FCC, CE and UL certifications where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	
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ORDERING OPTIONS

AMC534 – ABC – DEF – GHJ

A = FPGA DDR3 Memory

0 = None
1 = Reserved
2 = 4GB (total)

B = FPGA

0 = Reserved
1 = 5SGTC5
2 = 5SGTC7
3 = Reserved
4 = Reserved

C = Front Panel Size

1 = Reserved
2 = Mid-size
3 = Full-size

D = FPGA Transceiver PMA Speed Grade

1 = Highest
2 = Mid

E = FPGA Fabric Speed

1 = Highest
2 = Mid

F = FPGA PCIe Option

0 = No PCIe (ports 4-11)
1 = PCIe on ports 4-7
2 = PCIe on ports 8-11
3 = PCIe on ports 4-11

G = Clock Holdover Stability

0 = Standard (XO)
1 = Stratum-3 (TCXO)

H = Temperature Range

0 = Commercial (–5° to +55° C)
1 = Industrial (–20° to +70° C)
2 = Military (–40° to +85° C)*

J = Conformal Coating

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic

*Edge of module for conduction-cooled boards

RELATED PRODUCTS



VT899 Cube Chassis



FMC223 High Speed
FMC for DAC



UTC020 1000W Power
Module

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