AMC598

Quad DAC @ 12 GSPS with Quad ADC @ 3 GSPS, Kintex UltraScale AMC

AMC598

Key Features

- Xilinx UltraScale™ XCKU115 FPGA
- Quad ADC channels (AD9208) 14-bits @ 3 GSPS
- Quad DAC channels (AD9162 or AD9164) 16-bits @ 12 GSPS
- Two banks of 64-bit wide and a single bank of 32-bit wide DDR-4 for a total of 20 GB
- AMC Ports 4-11 are routed to FPGA per AMC.1, AMC.2 and AMC.4 (protocols such as PCIe, SRIO, 1/10/40GbE, etc. are FPGA programmable)
- AMC FCLKA, TCLKA, TCLKB, TCLKC and TCLKD are routed
- Clock Jitter cleaner
- Option for Direct RF Clock sampling for the ADC/DAC
- IPMI 2.0 compliant

Benefits

- Closely coupled ADC and DAC for low-latency response, dual channel for I/Q
- Sampling rate >6 GSPS for radar and EW applications
- Xilinx UltraScale™ XCKU115 FPGA provides powerful compute resource
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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AMC598

The AMC598 provides quad ADC with sample rates of up to 3 GSPS (AD9208) at 14-bits and a quad DAC (Analog Devices AD9162 or AD9164) with update rates of up to 12 GSPS and direct RF synthesis at 6 GSPS,16-bits making it suitable for signal capture/analysis applications such as COMINT/SIGINT, radar, research and instrumentation.

The unit has an on-board, re-configurable UltraScale™ XCKU115 FPGA which interfaces directly to ADC/DAC.

The FPGA has interface to a three banks of DDR4 memory channels (dual 64-bit wide and a single bank of 32-bit for a total of 20 GB). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The AMC598 comes with an 8HP panel size (it will occupy two mid-size slots in a chassis).

Block Diagram

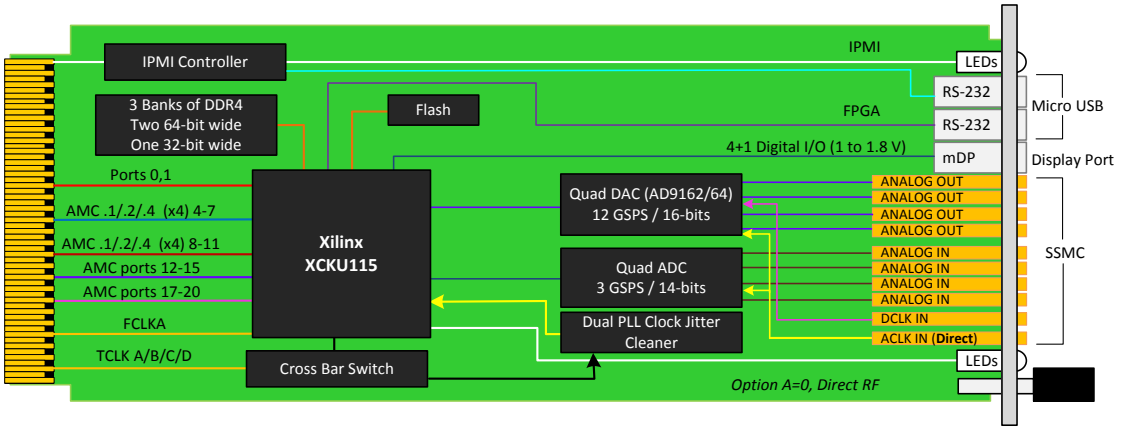


Figure 1: Functional Block Diagram for Option A = 0

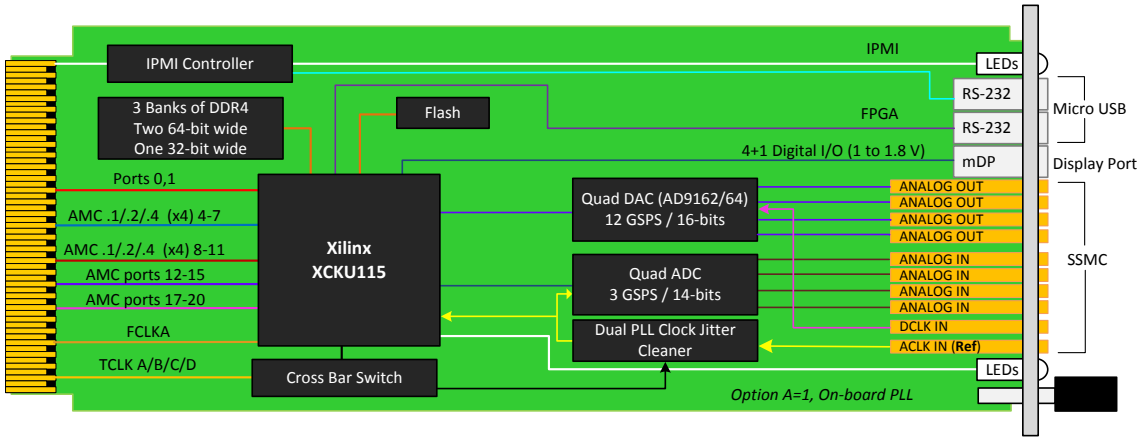


Figure 2: Functional Block Diagram for Option A = 1

Front Panel

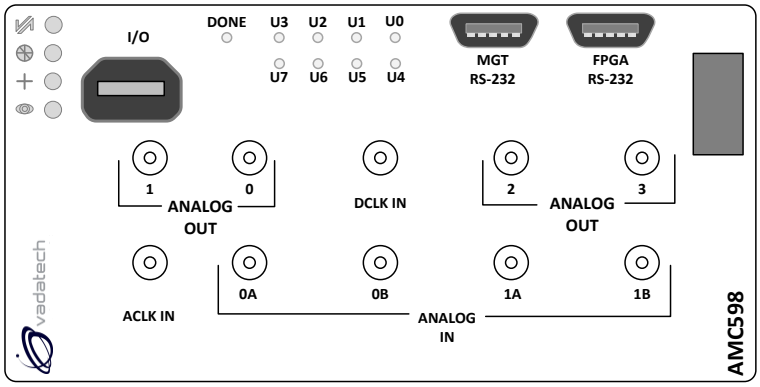


Figure 3: Front Panel for Option A=0

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

SUPPORTED SOFTWARE

Default FPGA image stored in flash memory

- Build Scripts
- Device Driver

Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tool for developing Digital Signal Processing (DSP) applications.

Xilinx Vivado Design Suite, Xilinx System Generator for DSP

DATA ACQUISITION

VadaTech offers a wide range of FPGA AMCs, RTMs, FMC Carriers and FMCs that can be combined to build a Data Acquisition (DAQ) sub-system. The DAQ Series™ software, when used with a supported hardware configuration, provides all that is needed to configure the system, acquire data and transfer it to a host processor. It also includes a user-configurable Graphical User Interface (GUI) which includes real-time display of acquired data. The host can be within the MTCA system or, via PCI113 or PCI123, in a separate PC. Full documentation is provided to allow users to customize system behavior or develop their own application on the AMC/FMC hardware.

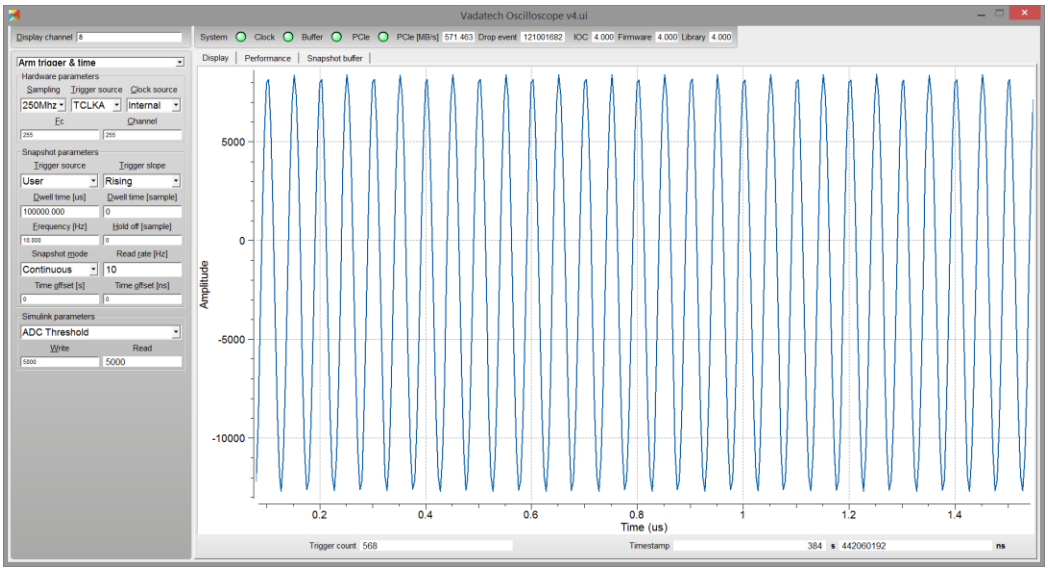
The DAQ includes data acquisition software that allows users to get up and running quickly and easily, while providing a high level of performance and allowing the user to extend functionality by adding their own FPGA code. Please contact VadaTech sales for the latest information on supported combinations of VadaTech hardware. (Note that the DAQ Series™ software is not currently supported for 3rd party hardware).

The DAQ Series™ software provides ability to easily implement system modelling and automatic code generation from Simulink® and MATLAB® (The Mathworks, Inc.) into Vivado FPGA project via System Generator® (Xilinx). This allows the programmer to interface with the hardware, program the FPGA at high level and benefit from:

- Vivado integration
- DSP modelling
- Bit and cycle accurate floating and fixed-point implementation
- Automatic code generation of VHDL or Verilog from Simulink
- Hardware co-simulation

Components provided in the DAQ Series™ software include:

- System libraries to configure clocking and triggers
- Sequencer to configure the acquisition (duration, start, stop)
- High-performance DMA firmware for acquiring ADC outputs and transferring to host processor
- Linux driver for host processor (e.g. AMC72x)
- EPICS channel access client API
- Pre-configured GUI (based on Qt Creator)



This software set allows the user to acquire, transfer and display data without the need for any user programming of the hardware. Status information is included in the GUI display, to ease integration and debugging activity.

The data acquisition software provided as part of the DAQ Series™ can be used as-delivered without the user needing to develop any FPGA code.

Full source code is provided for the libraries, sequencer, DMA, Linux driver and GUI, allowing users to easily customize or brand to their own requirements at the exception of a low level PCIe IP from Xilinx provided only as Netlist (this low level block doesn't require modification/customization from integrators or end-users).

Specifications

Architecture		
Physical	**Dimensions**	Single module, 8 HP
		Width: 2.89” (73.5 mm)
		Depth 7.11” (180.6 mm)
Type	**AMC FPGA ADC/DAC**	Xilinx UltraScale™ XCKU115 FPGA
		Three banks of DDR4 20GB total
		Quad ADC/ Quad DAC
Standards		
AMC	**Type**	AMC.1, AMC.2, and AMC.4 (FPGA programmable)
Module Management	**IPMI**	IPMI version 2.0
PCIe	**Lanes**	Dual x4 via FPGA to AMC
SRIO/XAUI	**Lanes**	Single or Dual x4 via FPGA to AMC
SerDes	**Lanes**	x8 via FPGA to AMC ports 12-15 and 17-20
Ethernet	**GbE and 10 GbE**	Dual GbE and 10/40 GbE
Configuration		
Power	**AMC598**	~70 W application dependent (may go up to 85 W)
Environmental	**Temperature**	Operating temperature: -5° to 45° C (55°C for limited time, performance restrictions may apply), industrial and extended versions also available (See environmental spec sheet)
		Storage Temperature: –40° to +85°C
	Vibration	Operating 9.8 m/s^2 (1G), 5 to 500Hz on each axis
	Shock	Operating 30G on each axis
	Relative Humidity	5 to 95 per cent, non-condensing
Front Panel	**Interface Connectors**	10x SSMC
		Micro USBs for MGT RS-232 and FPGA RS-232
		Mini DisplayPort for front panel I/O
	LEDs	IPMI management control
		8 user defined LEDs
	Mechanical	Hot-swap ejector handle
Software Support	**Operating System**	Agnostic
Conformal Coating		Humiseal 1A33 Polyurethane (Optional)
		Humiseal 1B31 Acrylic (Optional)
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of ATCA and µTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTM), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

AMC598 – ABC-DEF-GHJ

A = RF Direct Clock Sampling	D = Utilizing the ADC/DAC Nyquist Zones	G = Clock Holdover Stability
0 = Direct Clock 1 = On Board wide band PLL	0 = 1st/2nd 1 = 2nd/3rd	0 = Standard (XO) 1 = Stratum-3 (TCXO)
B = DAC	**E = FPGA Speed**	**H = ADC**
0 = Quad DAC Channels (AD9162) 1 = Quad DAC Channels (AD9164) 2 = No DAC 3 = Octal DAC Channels (AD9162) + 4 = Octal DAC Channels (AD9164) +	1 = Reserved 2 = High 3 = Highest *	0 = Quad ADC Channels (AD9208) 1 = Dual ADC Channels (AD9208) 2 = No ADC 3 = Octal ADC Channels (AD9208) ++
C = Front Panel Size	**F = PCIe Option ****	**J = Temperature Range and Coating**
1 = Reserved 2 = Reserved 3 = Reserved 4 = Reserved 5 = Reserved 6 = Reserved 7 = 8 HP 8 = 8 HP, MTCA.1 (captive screw both sides) 9 = 8 HP, Single Latching Flange	0 = No PCIe 1 = PCIe on ports 4 – 7 2 = PCIe on ports 8-11 3 = PCIe on ports 4 – 11 (x8 or dual x4 which requires a PCIe softcore for 8-11)	0 = Commercial (–5° to +55° C), No coating 1 = Commercial (–5° to +55° C), Humiseal 1A33 Polyurethane 2 = Commercial (–5° to +55° C),Humiseal 1B31 Acrylic 3 = Industrial (–20° to +70° C), No coating 4 = Industrial (–20° to +70° C), Humiseal 1A33 Polyurethane 5 = Industrial (–20° to +70° C), Humiseal 1B31 Acrylic 6 = Extended (–40° to +85° C), Humiseal 1A33 Polyurethane *** 7 = Extended (–40° to +85° C), Humiseal 1B31 Acrylic ***

Notes:

* Minimum Order Quantity applies for these FPGA SKU's.

** When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

*** Conduction cooled, temperature is at edge of module.

\+ Option H must be 2 (H=2) to select this option, Minimum Order Quantity applies.

++ Option B must be 2 (B=2) to select this option, Minimum Order Quantity applies.

Available Signal Bandwidth

Ordering Option (Number of Channels)	Interpolation (Minimum)	Maximum Fdata (MHz)	Available Signal Bandwidth (MHz)
Dual / Quad / Octal ADC (H = 0/1/3)	Bypass x1	3000	1500
Quad DAC (B = 0/1)	Bypass x1	Fdac = 5000	Fdac/2 = 2500
Octal DAC (B = 3/4)	Decimation x4	Fdac/4 = 1250	80% to 90% of 1250 (total I/Q)

Related Products

VT951

- MicroTCA rugged 1U 19” rackmount chassis platform
- Designed to meet MIL-STD-810F, MIL-STD-901D for shock/vibration
- Designed to meet MIL-STD-461E for EMI

FMC217

- ADC Option for ADC12DJ270 or ADC12DJ1600, 12-bit at 6.4 GSPS
- Wide full power bandwidth supports IF sampling of signals up to 6 GHz
- DAC AD9164/AD9162, 16-bit at 12 GSPS

AMC599

- Xilinx UltraScale™ XCKU115 FPGA
- Dual ADC @ 6.4 GSPS 12-bits or quad ADC at 3.2 GSPS
- Dual DAC (AD9162 or AD9164) @ 12 GSPS, 16-bits

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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