VPX516

FPGA FMC Carrier, 3U VPX, Virtex-7

VPX516

Conduction Cooled

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Key Features

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-46 and VITA-57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner
- VHDL reference design with source code
- Protocols such as PCIe, SRIO, 10GbE/40GbE, etc. are FPGA programmable
- Compatible with VadaTech and 3rd party FMCs
- 2.5 GB of DDR3 Memory
- Health Management through dedicated Processor

Benefits

- Reference design with VHDL source code speeds application development
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

OpenVPX™

VPX516

The VPX516 is a FPGA Carrier (VITA 46) with an FMC (VITA 57) interface. The unit has an on-board, re-configurable FPGA which interfaces directly to the FMC DP0-9 and all FMC LA/HA/HB pairs. The FPGA has interface to two DDR3 memory channels (64-bit wide and 16-bit wide). This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host. The 64-bit wide bank is 2GB and the 16-bit wide bank is 512 MB.

The module supports dual GbE and, dependent on FPGA code loaded, PCIe up to Gen3 (dual x4 or x8 lane), or dual SRIO, 10GbE or 40GbE on P1. In addition, from the FPGA going to the P1 there are dual GTX that could be used as SATA or any other protocols. Additional x4 lanes are brought out to P2 for direct FPGA-to-FPGA connection using lightweight protocols such as Aurora (backplane dependent).

The VPX516 provide health management through the dedicated management processor (including temp, voltage, FRU info, etc.).

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA-47, up to V3 and OS2.

Figure 1: Air Cooled

Figure 2: Conduction Cooled

Block Diagram

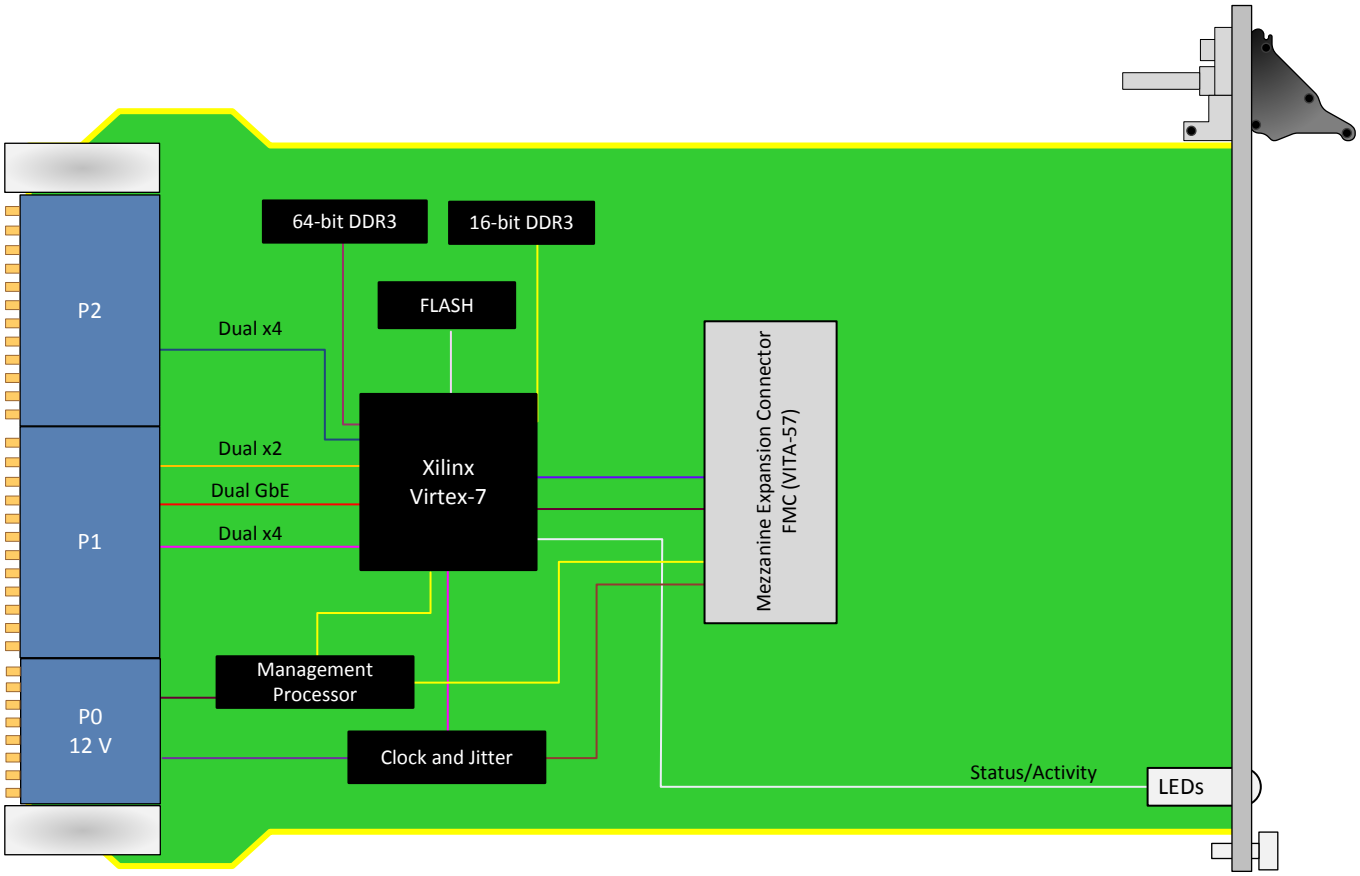

Figure 3: Functional Block Diagram

Front panel

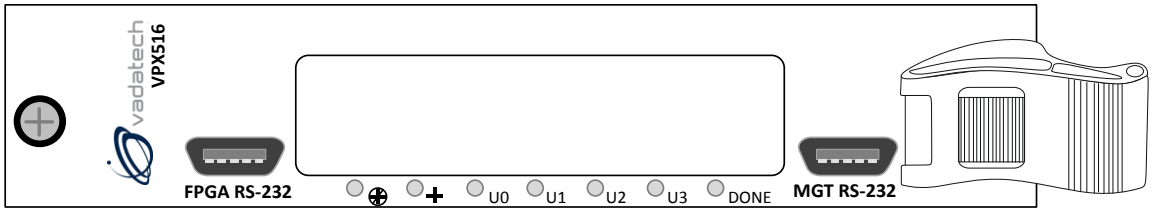

Figure 4: Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tool for developing Digital Signal Processing (DSP) applications.

Xilinx Vivado Design Suite, Xilinx System Generator for DSP

Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Configuration		
Power		~40 W (dependent on FPGA load and FMC)
Front Panel	**FMC**	Single FMC slot
	Micro USB	RS-232 from Health Management CPU and RS-232 from FPGA
	LEDs	User defined by the FPGA and Health Management
On-board Interfaces		
VPX Interfaces	**Slot Profiles**	See ordering options
	Rear IO	Dual x4 fabric on P1 (PCIe Gen3 /10GbE/40GbE/ SRIO per FPGA load)
		Dual GbE on P1
		Dual x4 fabric on P2
	Power Supplies	On P0: VS1 = 12 V
		Aux voltage for the management processor
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of ATCA and µTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTM), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX516– 0BC-DEF-GHJ

	D = FPGA Speed	G = Applicable Slot Profiles
	0 = Reserved 1 = High 2 = Highest	0 = 5 HP
B = Expansion Plane (P2)	**E = Clock Holdover Stability**	**H = Environmental**
0 = Not routed 1 = Routed (x8 SERDES to the P2)	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification table option H description
C = FPGA	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = Reserved 1 = Reserved 2 = XC7VX690T	0 = None 1 = PCIe / None 2 = None / PCIe 3 = PCIe / PCIe	0 = None 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H=4**
Operating Temperature	AC1* (0°C to +55°C	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

* Nomenclature per ANSI / VITA-47. Contact local sales office for conduction cooled (H=2, 3, 4).

Related Products

FMC214

- Dual complete transceiver signal chain solution using Analog Devices AD9361 transceiver
- Frequency range 70 MHz to 6 GHz with instantaneous bandwidth from 200 kHz to 56 MHz
- MIMO transceiver is Time Domain Duplex (TDD) and Frequency Domain Duplex (FDD) compatible

FMC225

- FPGA Mezzanine Card (FMC) per VITA 57
- TI ADC12J4000 ADC
- Analog Devices AD9129 DAC

FMC226

- FPGA Mezzanine Card (FMC) per VITA 57
- Dual Texas Instruments ADC12J4000 ADC
- Supported by DAQ Series™ data acquisition software

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ALLIANCE PROGRAM
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