VPX585

Zynq UltraScale+ FPGA, FMC+ Carrier, VPX

Key Features

- Xilinx UltraScale+ XCZU19EG FPGA
- Single FMC+ (VITA 57.4) site
- 8 GB of 64-bit wide DDR-4 Memory (single bank) with ECC (CPU)
- 8 GB of 64-bit wide DDR-4 Memory (single bank, FPGA)
- MPSoC with block RAM and UltraRAM
- SD Card (option)
- 128 MB of boot Flash
- 64 GB of user Flash

Benefits

- FMC+ site on a single module VPX
- Zynq UltraScale+ MPSoC
- Electrical, mechanical, software, and system-level expertise in house
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX585

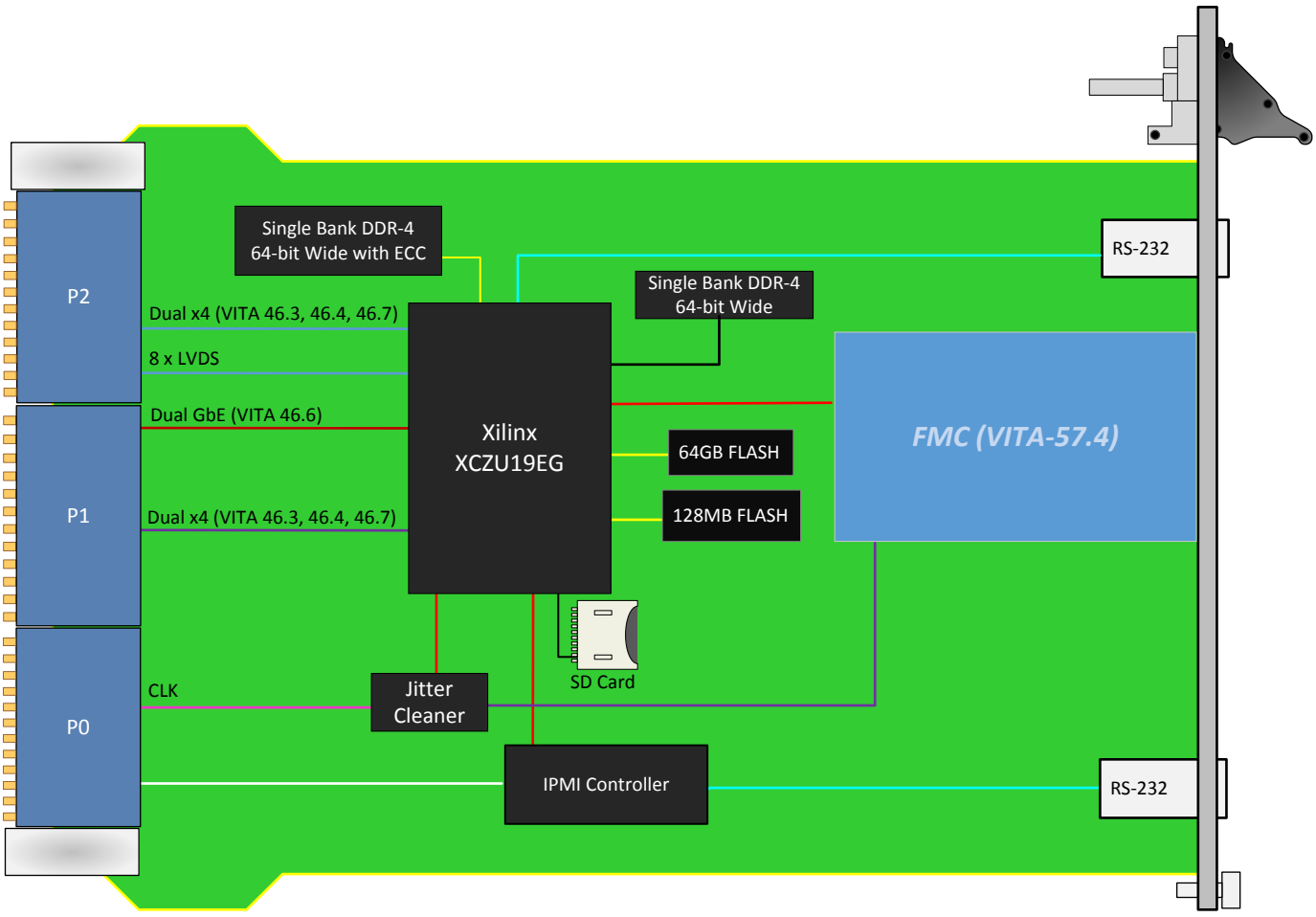
The VPX585 is a 3U VPX FPGA Carrier with single FMC+ (VITA-57.4) interface. The unit has an on-board, re-configurable FPGA which interfaces directly to the VPX P1 connector and all FMC+ LA/HA/HB pairs (the module does not support HSPCe connector).

The FPGA has interface to a single DDR4 memory channel (64-bit wide with ECC to the ARM CPU). In addition there is 64GB of DDR-4 memory channel that connects to the FPGA. This allows for large buffer sizes to be stored during processing as well as for queuing the data to the host.

The VPX is based on Xilinx UltraScale+ XCZU19EG MPSoC FPGA with single FMC+ site. The FPGA has 1968 DSP Slices and 1143k logic cells. The XCZU19EG includes quad-core ARM application processor, dual-core ARM real-time processor and Mali™ graphics processing unit, as well as over 34.6 Mb of block RAM and 36 Mb of UltraRAM.

The module has on board 64 GB of Flash, 128 MB of boot flash and an SD Card as an option.

Block Diagram



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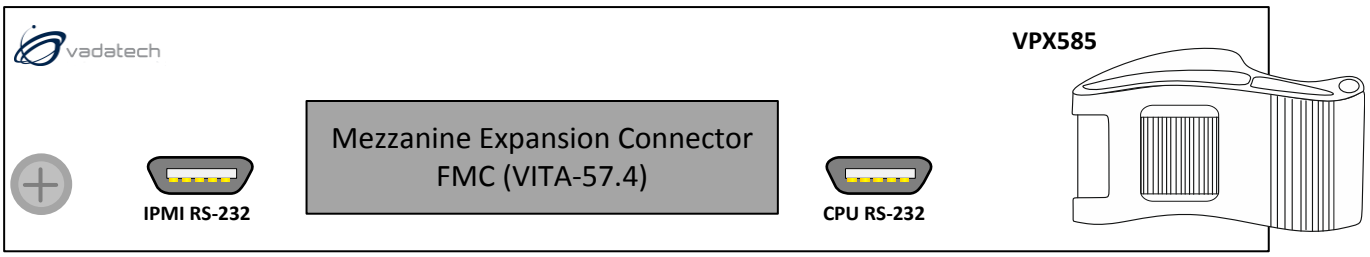
Front Panel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VPX585
Mezzanine Expansion Connector
FMC (VITA-57.4)
IPMI RS-232
CPU RS-232

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REFERENCE DESIGN

VadaTech provides several Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and 3U Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is geared to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate:

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provide reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is royalty free to use and modify on VadaTech products but customers are restricted from redistributing the reference code and use of this code for any other purpose.

The reference VHDL is shipped in one or more files based on number of ordering options. Not all ordering option have an impact on the FPGA and a new image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

SUPPORTED SOFTWARE

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The design pre-compiled images make use of hardware evaluation licenses, where necessary, instead of full license. VadaTech does not provide license for the Vivado tool or Xilinx IP cores, please contact Xilinx for more information.

Xilinx also provides System Generator tool for developing Digital Signal Processing (DSP) applications.

Xilinx Vivado Design Suite, Xilinx System Generator for DSP

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Specifications

Architecture		
Physical	**Dimensions**	3U, 1” pitch
Type	**FPGA**	Xilinx Zynq UltraScale+ with FMC+ site
Configuration		
Power	**VPX585**	~30W FPGA load dependent and no FMC+
Front Panel	**Interface Connectors**	Single FMC+ Slot
		Dual micro USB for RS-232 (management and CPU)
On-board Interfaces		
VPX Interfaces	**Slot Profiles**	See ordering options
	Rear IO	CLK on P0
		Dual x4 fabric (VITA 46.3, 46.4, 46.7) on P1
		Dual GbE (VITA 46.6) on P1
		Dual x4 fabric (VITA 46.3, 46.4, 46.7) on P2
		8 x LVDS on P2
Software Support	**Operating System**	Linux
Other		
MTBF	MIL Hand book 217-F@ TBD hrs	
Certifications	Designed to meet FCC, CE and UL certifications, where applicable	
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards	
Warranty	Two (2) years	

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of ATCA and µTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTM), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

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Ordering Options

VPX585– 0BC-DEF-GHJ

	D = FPGA Speed	G = Applicable Slot Profiles
	1 = Reserved 2 = High 3 = Highest	0 = 5 HP
B = Expansion Plane (P2)	**E = Clock Holdover Stability**	**H = Environmental**
0 = Not routed 1 = Dual x4	0 = Standard (XO) 1 = Stratum-3 (TCXO)	See Environmental Specification table option H description
C = SD Card	**F = PCIe Option (P1) for Data Port 1/2**	**J = Conformal Coating**
0 = None 1 = 32 GB	0 = None 1 = PCIe / None 2 = None / PCIe 3 = PCIe / PCIe	0 = None 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

* When the ports are not PCIe the lanes are electrically compatible with SRIO, XAUI, and other SerDes protocols.

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H=4**
Operating Temperature	AC1* (0°C to +55°C	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

* Nomenclature per ANSI / VITA-47. Contact local sales office for conduction cooled (H=2, 3, 4).

Related Products

VPX592

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA-46 and VITA-57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

Contact

VadaTech Corporate Office

198 N. Gibson Road, Henderson, NV 89014
Phone: +1 702 896-3337 | Fax: +1 702 896-0332

Asia Pacific Sales Office

7 Floor, No. 2, Wenhu Street, Neihu District, Taipei 114, Taiwan
Phone: +886-2-2627-7655 | Fax: +886-2-2627-7792

VadaTech European Sales Office

VadaTech House, Bulls Copse Road, Southampton, SO40 9LR
Phone: +44 2380 016403

info@vadatech.com | www.vadatech.com

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