VPX550

Kintex UltraScale™ with COM Express, 6U VPX

VPX550

Key Features

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- COM Express Module Type-6
- 8 GB of DDR-4 Memory to FPGA
- CFAST socket for removable storage
- Health Management through dedicated Processor

Benefits

- XCKU115 FPGA provides 5,520 DSP slices for complex processing
- Reference design with VHDL source code speeds application development
- Full system supply from industry leader
- AS9100 and ISO9001 certified company

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VPX550

The VPX550 is a 6U VPX board with Kintex UltraScale™ FPGA and a COM Express module.

The on-board FPGA is a Kintex UltraScale™ with 8 GB of DDR-4 Memory. The FPGA provides JTAG, USB (USB to RS-232) and RS-232 to the front panel with status LEDs.

The FPGA provide extensive I/O to the rear:

- 1x GbE as 1000Base-TX and 2x SERDES on P1
- 16x SERDES on P2
- 152 signals routed through P3, P4, P5 and P6

The VPX550 has the option for a COM Express Type-6. The COM Express provides dual USB 3.0, HDMI, GbE (as 1000Base-TX), USB 3.0 and status LEDs to the front panel. The front panel has a CFAST socket for removable storage which is routed to the Com-Express Module.

The COM Express module connects to the FPGA via PCIe Gen3 x4.

The health management is based on the VITA 46.11.

The unit is available in a range of temperature and shock/vib specifications per ANSI/VITA 47, up to V3 and OS2.

Please contact VadaTech for details of Conduction Cooled versions.

Figure 1: VPX550 Front View

Block Diagram

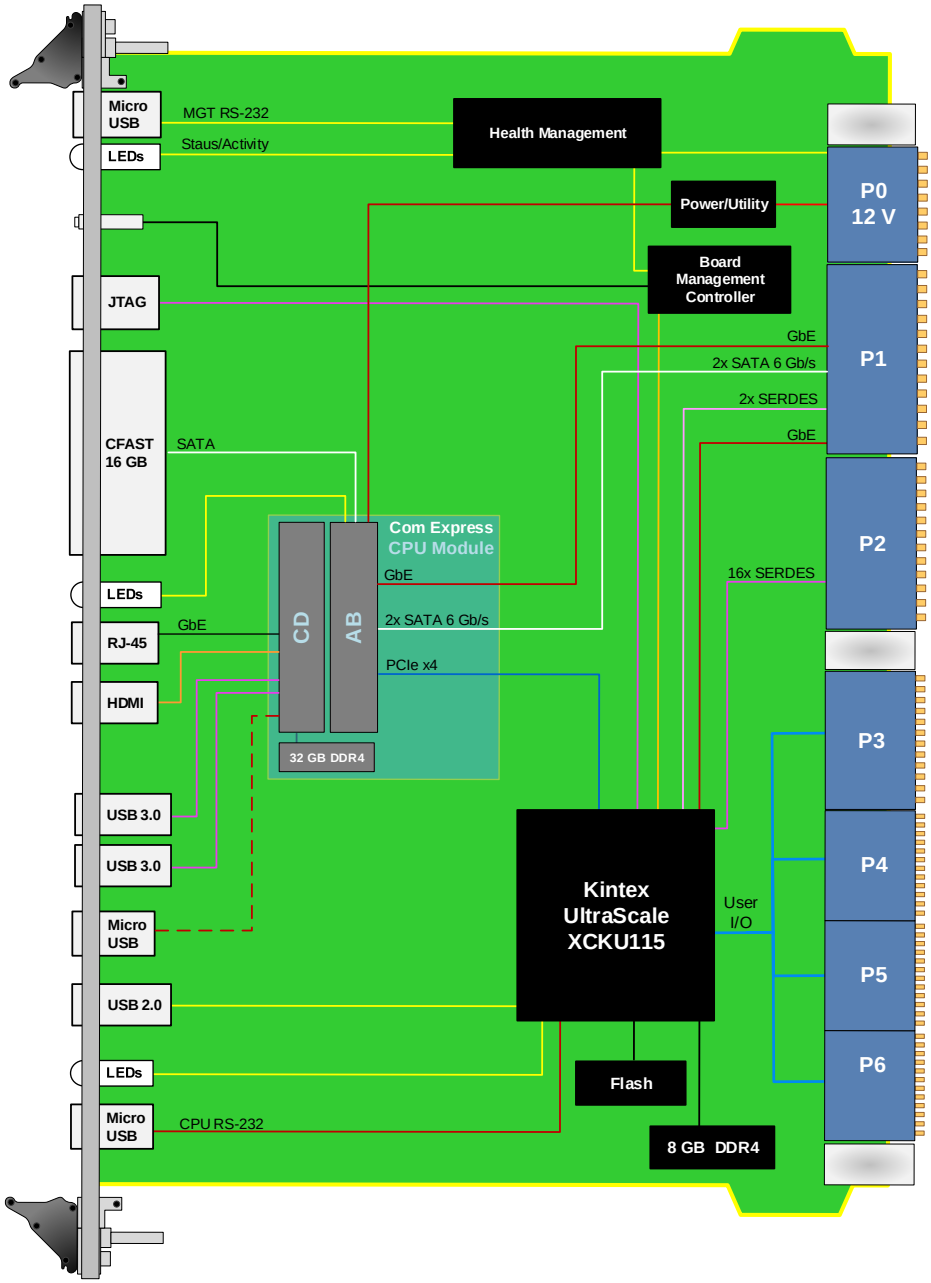

Figure 2: VPX550 Functional Block Diagram

Front Panel

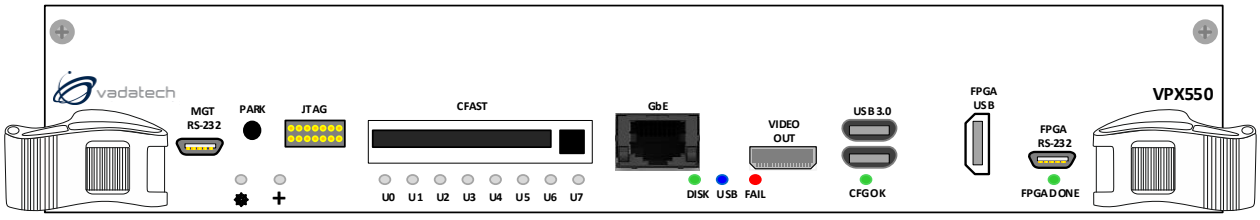

Figure 3: VPX550 Front Panel

Reference Design

VadaTech provides an extensive range of Xilinx based FPGA products. The FPGA products are in two categories; FPGA boards with FMC carriers and FPGA products with high speed ADC and DACs. The FPGA products are designed in various architectures such as AMC modules, PCIe cards and Open VPX.

VadaTech provides a reference design implementation for our FPGAs complete with VHDL source code, documentation and configuration binaries. The reference design focuses on the I/O ring of the FPGA to demonstrate low-level operation of the interconnections between the FPGA and other circuits on the board and/or backplane. It is designed to prove out the hardware for early prototyping, engineering/factory diagnostics and customer acceptance of the hardware, but it does not strive to implement a particular end application. The reference VHDL reduces customer time to develop custom applications, as the code can be easily adapted to meet customer's application requirements.

The reference design allows you to test and validate the following functionality (where supported by the hardware):

- Base and Fabric channels
- Clocks
- Data transfers
- Memory
- User defined LEDs

Xilinx provides Vivado Design Suite for developing applications on Xilinx based FPGAs. VadaTech provides reference VHDL developed using the Vivado Design Suite for testing basic hardware functionality. The reference VHDL is provided royalty free to use and modify on VadaTech products, so can be used within applications at no additional cost. However, customers are restricted from redistributing the reference code and from use of this code for any other purpose (e.g. it should not be used on non-VadaTech hardware).

The reference VHDL is shipped in one or more files based on a number of ordering options. Not all ordering options have an impact on the FPGA and a new FPGA image is created for those options that have direct impact on the FPGA. Use the correct reference image to test your hardware. For more information, refer to the FPGA reference design manual for your device which can accessed from customer support site along with the reference images.

Supported Software

- Default FPGA image stored in flash memory
- Linux BSP
- Build Scripts
- Device Driver
- Reference application projects for other ordering options

The user may need to develop their own FPGA code or adapt VadaTech reference code to meet their application requirements. The supplied pre-compiled images may make use of hardware evaluation licenses, where necessary, instead of full licenses. This is because VadaTech does not provide licenses for the Vivado tool or Xilinx IP cores, so please contact Xilinx where these are required.

Xilinx also provides System Generator tools for developing Digital Signal Processing (DSP) applications.

See the following links:

Xilinx Vivado Design Suite, Xilinx System Generator for DSP.

Specifications

Architecture		
Physical	**Dimensions**	6U, 5HP or 10HP depending on the Com-Express Module
FPGA		Xilinx Kintex UltraScale™ XCKU115, 8 GB DDR4
COM Express		Type-6
Configuration		
Power	**VPX550**	~80 W (Com Express and FPGA load dependent)
Front Panel	**JTAG**	Standard JTAG header
	Micro USB	RS-232 from FPGA and RS-232 from Health Management
	RJ-45	GbE
	HDMI	1.2
	USB	2 of USB 3.0 Type A 1 of USB 2.0 Type A (to FPGA for RS-232)
	LEDs	CPU Fail (Red), from Com Express module Disk (Green), from Com Express module USB (Blue), from Com Express module User defined by the FPGA and Health Management
	CFAST	w/retention
	Switch	Push-button
On-board Interfaces		COM Express Module
VPX Interfaces	**Slot Profiles**	See ordering options
	Rear IO	P1: GbE and dual SATA to CPU GbE and 2x SERDES to FPGA
		P2: 16x SERDES from FPGA
		P3 to P6: user I/O to RTM
	Power Supplies	On P0: VS1 = 12 V

Other	
MTBF	MIL Hand book 217-F@ TBD hrs
Certifications	Designed to meet FCC, CE and UL certifications, where applicable
Standards	VadaTech is certified to both the ISO9001:2000 and AS9100B:2004 standards
Warranty	Two (2) years

INTEGRATION SERVICES AND APPLICATION-READY PLATFORMS

VadaTech has a full ecosystem of OpenVPX, ATCA and MTCA products including chassis platforms, shelf managers, AMC modules, Switch and Payload Boards, Rear Transition Modules (RTMs), Power Modules, and more. The company also offers integration services as well as pre-configured Application-Ready Platforms. Please contact VadaTech Sales for more information.

Ordering Options

VPX550 – 000-DEF-GHJ

	D = FPGA Speed	G = Applicable Slot Profiles
	1 = Reserved 2 = High 3 = Highest	0 = 5 HP 1 = 10 HP, VITA 48.1
	E = CFAST	**H = Environmental**
	0 = None 1 = 16 GB	See Environmental Specification Table below
	F = Com Express	**J = Conformal Coating**
	0 = Com Express-SL AdLink Core i-7 1 = None 2 = Reserved 3 = Reserved	0 = None 1 = Humiseal 1A33 Polyurethane 2 = Humiseal 1B31 Acrylic

Environmental Specification

	Air Cooled		Conduction Cooled		
Option H	**H = 0**	**H = 1**	**H = 2**	**H = 3**	**H = 4**
Operating Temperature	AC1* (0°C to +55°C)	AC3* (-40°C to +70°C)	CC1* (0°C to +55°C)	CC3* (-40°C to +70°C)	CC4* (-40°C to +85°C)
Storage Temperature	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C1* (-40°C to +85°C)	C3* (-50°C to +100°C)	C3* (-50°C to +100°C)
Operating Vibration	V2* (0.04 g2/Hz max)	V2* (0.04 g2/Hz max)	V3* (0.1 g2/Hz max)	V3* (0.1 g2/Hz max)	V3 (0.1 g2/Hz max)
Storage Vibration	OS1* (20g)	OS1* (20g)	OS2* (40g)	OS2* (40g)	OS2* (40g)
Humidity	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing	95% non-condensing

Notes: *Nomenclature per ANSI/VITA 47. Contact local sales office for conduction cooled (H = 2, 3, 4).

Related Products

VPX516

- 3U FPGA carrier for FPGA Mezzanine Card (FMC) per VITA 46 and VITA 57
- Xilinx Virtex-7 690T FPGA in FFG-1761 package
- High-performance clock jitter cleaner

VPX592

- 3U FPGA carrier for FMC per VITA 46 and VITA 57
- Xilinx Kintex UltraScale™ XCKU115 FPGA
- High-performance clock jitter cleaner

VPX599

- Xilinx Kintex UltraScale™ XCKU115 FPGA
- Dual ADC @ 6.4 GSPS 12-bits
- Dual DAC @ 12 GSPS 16-bits (AD9162 or AD9164)

Contact

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DOC NO. 4FM737-12 REV 01 | VERSION 1.2 – MAY/18