General Standards Corporation

High Performance Bus Interface Solutions

PMC66-16AISS16AO2

16-Bit, 18-Channel, 1.0 MSPS PMC Analog Input/Output Board

With 16 Simultaneously Sampled Analog Inputs, and Two Analog Outputs

Available also in PCI, cPCI and PC104-*Plus* form factors as:

PCI66-16AISS16AO2:	**PCI**, short length
cPCI66-16AISS16AO2:	**cPCI,** 3U
PC104P66-16AISS16AO2:	**PC104-*Plus***

See Ordering Information for details.

FEATURES:

- **Analog Inputs:**
  - 16 Differential Analog Inputs with Dedicated 16-Bit SAR ADC per Channel
  - True Simultaneous Input Sampling to 1.0 MSPS per channel
  - SAR Architecture; No Minimum Sample Rate
- **Analog Outputs:**
  - Two Single-Ended Analog Outputs with Dedicated 16-Bit DAC per Channel
  - Simultaneous Output Clocking Rates to 1.0 MSPS per Channel
  - Selectable Direct-Write or FIFO-Buffered Access
  - Buffer Configurable as Open for Data Streaming, or Circular for Periodic Functions
- **Common Analog I/O Features:**
  - Software-Selectable Input/Output Ranges: ±10V, ±5V, ±2.5V
  - Independent 256-Ksample Input and Output FIFO Data Buffers
  - Independent or synchronous input/output clocking
  - Hardware Clock and Sync I/O for Multiboard Operation
  - Internal Power Conversion; Single 5-Volt PCI Power Requirement
  - DMA Engine Minimizes Bus Congestion
  - Timing Controlled by Internal Rate Generator, by Software Clocking, or Externally
  - Three Independent 24-Bit frequency dividers.
  - Internal Autocalibration
- Six Bidirectional Digital I/O lines
- 66 MHz 32-Bit PCI Support, with Universal 5V/3.3V Signaling
- Single-Width PMC Form Factor with Integral EMI Shield.

TYPICAL APPLICATIONS:

- ✓ High Performance Data Acquisition
- ✓ Arbitrary Waveform Generation
- ✓ Event Capture
- ✓ Ultrasound
- ✓ Robotics
- ✓ Positioning Systems

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FUNCTIONAL DESCRIPTION

The 16-Bit PMC-16AISS16AO2 analog I/O module samples and digitizes 16 input channels simultaneously at rates up to 1.0 million samples per second per channel, and the resulting 16-bit sampled data is available to the PCI bus through a 256K-Sample FIFO buffer. Sampling can be controlled in groups of 1 through 16 channels, and the sample clock can be generated either from an internal rate generator, or by software or an external source. Both burst and continuous sampling modes are supported, and input ranges are software-selectable as ±10V, ±5V or ±2.5V. The inputs are divided into two channel groups, with an independent software-controlled range assignable to each group.

Two analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V that are independent of the input range assignments. The outputs are accessed either directly through two dedicated control registers, or through a 256K-Sample FIFO buffer for waveform generation. Six bidirectional digital I/O lines are programmable as inputs or outputs. Output clocking can be synchronized to analog input sampling.

On-demand autocalibration determines and applies offset and gain correction values for all input and output channels. A selftest input switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host.

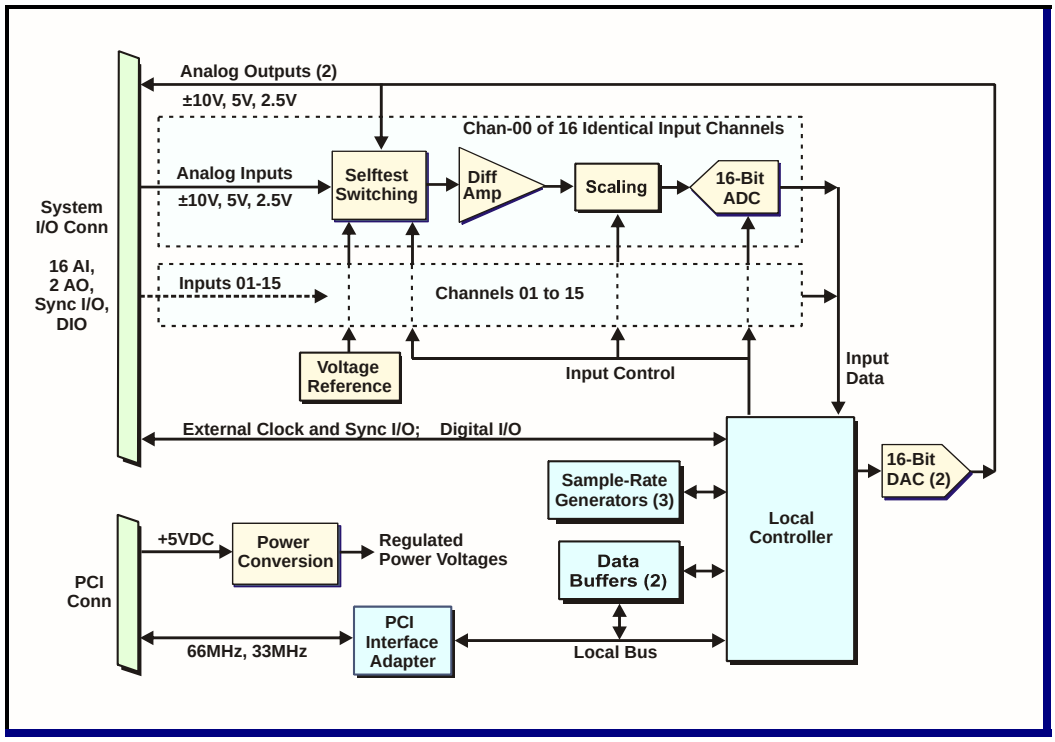

Figure 1. PMC-16AISS16AO2; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. All operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional air cooling.

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PERFORMANCE SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

Analog Input Characteristics:

Configuration:	16 differential analog input channels; Dedicated 16-Bit ADC per channel. Optional 8-Channel version available.
Voltage Ranges:	Independently assignable between two groups of input channels as: ±10V, ±5V or ±2.5V full scale.
Input Impedance:	2 Megohms Line-Line in parallel with 40pF.
Bias Current:	300 nanoamps typical, all ranges
Crosstalk Rejection:	84dB, DC-10kHz. 70dB at 100kHz.
Signal/Noise Ratio (SNR):	82 dB typical; 10Hz - 500kHz
Common Mode Rejection:	70dB DC-10kHz; 50dB at 500kHz. Typical with CMV = ±10V, Vin = Zero.
Overvoltage Protection:	±25V with power applied, ±15 Volts with power removed.

Analog Input Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Sample Rate:	Zero to 1.0 MSPS per channel.
Sampling Mode::	Simultaneous; Successive-approximation conversion, all active inputs.
DC Accuracy: (Maximum composite error after autocalibration)	Range ±10V: Midscale Accuracy ± 2mV, Fullscale Accuracy ± 5mV Range ±5V: Midscale Accuracy ± 1mV, Fullscale Accuracy ± 3mV Range ±2.5V: Midscale Accuracy ± 0.8mV, Fullscale Accuracy ± 2mV
Small Signal Bandwidth:	Zero to 1.3MHz, -3dB, all ranges
Settling Time:	5us to 0.1%; halfscale step; typical; all ranges.
Power Bandwidth:	2.2 Vpp-MHz; -3dB
Integral Nonlinearity:	±0.007 percent FSR (FSR = fullscale range; e.g.: 20V on ±10Vrange).
Differential Nonlinearity:	±0.003 percent FSR.

Analog Input Operating Modes and Controls

Input Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Hardware Clock I/O, Software clock.
Sampling Modes:	Continuous sampling, and triggered burst.
Internal Rate Generators:	Two independent rate generators, one for ADC clocking; one for burst triggering. Both programmable from 3-1,000,000 sample clocks per second, using 24-Bit dividers from the master clock frequency.
External Clock I/O:	TTL, bidirectional. Zero to 1,000,000 sample clocks per second.
Principal Status Register:	Consolidates critical status flags at a single Longword location.
Input Data Format:	16 Bits. Selectable as offset binary or two's complement. First-channel and end of-burst tagged.

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Analog Output Characteristics:

Configuration:	Two single-ended output channels. (Ordering option)
Voltage Ranges:	±10, ±5 or ±2.5 Volts; Independent of analog input ranges.
Output Resistance:	1.0 Ohm maximum at I/O connector pins.
Output protection:	Withstands sustained short-circuiting to ground
Load Current:	Zero to ±3ma per channel
Load Capacitance:	Stable with any load capacitance
Noise:	1.0mV-RMS, 10Hz-100KHz typical
Glitch Impulse:	7 nV-s, typical on ±5V range

Analog Output Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)		
Output Access:	Direct register access or 256K-Sample FIFO buffer.		
DC Accuracy:	Range	Midscale Accuracy	±Fullscale Accuracy
(Max error, no-load)	±10V	±4mV	±8mV
	±5V	±2mV	±6mV
	±2.5V	±1.5mV	±4mV
Settling Time:	3us to 0.1 percent, typical with halfscale step, no-load.		
Crosstalk Rejection:	70 dB minimum, DC-100 kHz		
Integral Nonlinearity:	±0.007 percent of FSR, maximum		
Differential Nonlinearity:	±0.002 percent of FSR, maximum		

Analog Output Operating Modes and Controls

Output Data Buffer:	256K-sample FIFO
Sample Clock Sources:	Internal rate generator; External Clock I/O, Software clock. 1MHz max.
Burst Triggering Sources:	TTL external Trigger I/O (shared with analog inputs), Software trigger.
Clocking Modes:	Continuous or periodic clocking, and triggered burst.
Internal Rate Generator:	Programmable from 3-1,000,000 output clocks per second. Divides Master Clock frequency to clocking rate using a 24-bit divider.
External Clock I/O:	TTL, bidirectional. Zero to 1,000,000 sample clocks per second.
Output Data Format:	16-Bits. Selectable as offset binary or two's complement.

Digital Input/Outputs:

Six TTL I/O lines, individually configurable as inputs or outputs. 0.2ma maximum input loading as current source, 4ma output loading as either sink or source. Direct register control.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33/66MHz, universal (5V/3.3V) signaling, Supports block-mode and demand-mode DMA data transfers in two channels as bus master.

Power Requirements

+5VDC ±0.25 VDC at 1.3 Amp typical, 1.5 Amp maximum.

Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

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PHYSICAL PARAMETERS

Mechanical Characteristics *

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)
Shield: Side-1 is protected by an EMI shield.

* Mechanical dimensions are shown for the native single-width PMC form factor. See Ordering Information.

Environmental Specifications

Ambient Temperature Range:	Operating 0 to +65 Degrees Celsius inlet air: Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional air cooling; 150 LFPM

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number **PMC66-16AISS16AO2-16-2-45.00M** describes a PMC module with 16 input channels, two output channels, a 45MHz master clock frequency, and no custom features.

Basic Model Number	Form Factor
PMC66-16AISS16AO2	**PMC** (Native)
PCI66-16AISS16AO2 *	**PCI, short length**
cPCI66-16AISS16AO2 *	**cPCI, 3U**
PC104P66-16AISS16AO2 **	**PC104-*Plus***

* PMC module installed and tested on an adapter, with mechanical and functional equivalency.
** PMC module installed and tested on an adapter, with functional equivalency.
Contact factory for availability in native form factors.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	**16 Input Channels**	**A = 16**
	8 Input Channels	**A = 8**
Number of Output Channels	**2 Output Channels**	**B = 2**
	No Analog Outputs	**B = 0**
Master Clock Frequency *	**45.000MHz**	**C = 45.000M**
Custom Feature	**---**	**D ****

* Custom frequencies available from 44-47MHz. Contact Sales for details.
** Numeric code determined by specific feature. Blank or zero (0) if no custom feature applies.

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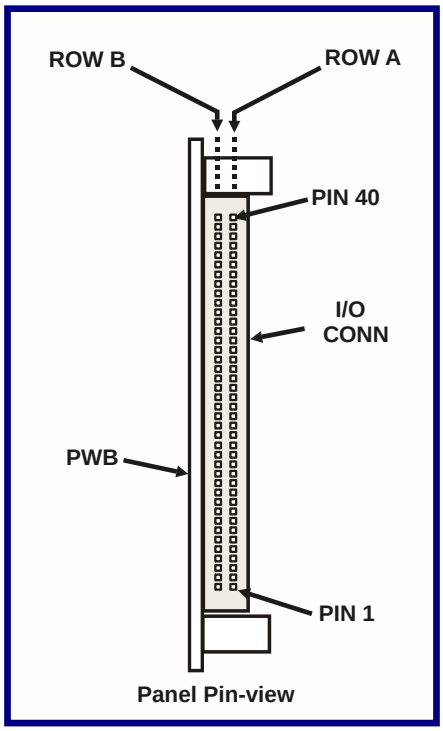
SYSTEM INTERFACE CONNECTOR

Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	INP00 LO *
2	INP00 HI *
3	INPUT RTN
4	INPUT RTN
5	INP01 LO *
6	INP01 HI *
7	INPUT RTN
8	INPUT RTN
9	INP02 LO **
10	INP02 HI **
11	INPUT RTN
12	INPUT RTN
13	INP03 LO **
14	INP03 HI **
15	INPUT RTN
16	INPUT RTN
17	INP04 LO *
18	INP04 HI *
19	INPUT RTN
20	INPUT RTN
21	INP05 LO *
22	INP05 HI *
23	INPUT RTN
24	INPUT RTN
25	INP06 LO **
26	INP06 HI **
27	INPUT RTN
28	INPUT RTN
29	INP07 LO **
30	INP07 HI **
31	INPUT RTN
32	INPUT RTN
33	INP08 LO *
34	INP08 HI *
35	INPUT RTN
36	INPUT RTN
37	INP09 LO *
38	INP09 HI *
39	OUTPUT RTN
40	ANA OUT 00

ROW-B	
PIN	SIGNAL
1	INP10 LO **
2	INP10 HI **
3	INPUT RTN
4	INPUT RTN
5	INP11 LO **
6	INP11 HI **
7	INPUT RTN
8	INPUT RTN
9	INP12 LO *
10	INP12 HI *
11	INPUT RTN
12	INPUT RTN
13	INP13 LO *
14	INP13 HI *
15	INPUT RTN
16	INPUT RTN
17	INP14 LO **
18	INP14 HI **
19	INPUT RTN
20	INPUT RTN
21	INP15 LO **
22	INP15 HI **
23	OUTPUT RTN
24	ANA OUT 01
25	DIGITAL RTN
26	DIO 00
27	DIGITAL RTN
28	DIO 01
29	DIGITAL RTN
30	DIO 02
31	DIGITAL RTN
32	DIO 03
33	DIO 04
34	DIO 05
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	TRIGGER I/O
39	DIGITAL RTN
40	INPUT CLK I/O

* Input Group-A. ** Input Group-B.
The 8 input-channel configuration contains input Channels 00-07.



System Mating Connector:
Standard 80-pin 0.050" dual-ribbon socket:
Robinson Nugent **P50E-080S-TG,** or equivalent

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