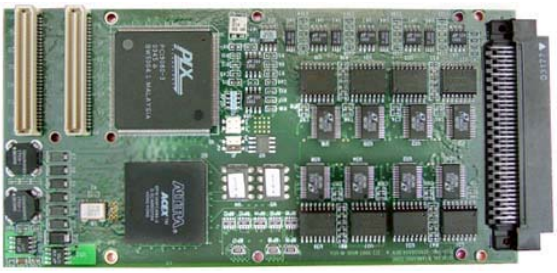
PMC-12AISS44AO4

12-Channel, 12-Bit PMC Analog Input/Output Board

With Eight Simultaneously-Sampled Wide-Range Inputs at 2.0 MSPS per Channel, Four Analog Outputs, and 16-Bit Digital I/O Port



FEATURES

- **8 Differential Analog Inputs with Dedicated 12-Bit, 2.0 MSPS ADC per Channel**
  - **True Simultaneous Sampling of all Inputs; Minimum Data Skew**
  - **Sampling Rates to 2.0 MSPS per Channel (16 MSPS Aggregate Rate)**
  - **Two Input Range Groups; Each Factory Configured as ±100mV, ±1V or ±10V**
  - 64-Ksample Analog Input FIFO Data Buffer
  - Supports Two DMA Channels in Block-Mode or Demand-Mode
- **4 Analog Output Channels with Direct Register Access**
- **16-Bit Bidirectional Digital I/O Port**
- Sampling Controlled by Internal Rate Generator, by Software Trigger, or Externally
- On-Demand Internal Autocalibration
- Hardware Sync I/O for Multiboard Operation
- Full Power Bandwidth to 900kHz at 4Vp-p; to 220kHz at 20Vp-p
- Conforms to PCI Local Bus Specification, Revision 2.3, with Universal Signaling
- Single-width PMC Form Factor

APPLICATIONS

- **Wideband Analog Inputs**
- **Low-Level Inputs**
- **Instrumentation**
- **Transducer Inputs**
- **Event Capture**
- **Acoustic Sensor Inputs**
- **Dynamic Test Systems**
- **Voltage Control**
- **Closed-Loop Systems**

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FUNCTIONAL DESCRIPTION

The 12-Bit PMC-12AISS44AO4 analog I/O board samples and digitizes eight input channels simultaneously at rates up to 2.0 million samples per second for each channel. 12-bit sampled data is available to the PCI bus through a 64K-Sample FIFO buffer. All data is channel-tagged.

Analog input sampling can be controlled from an internal rate generator, through software, or by external hardware. Both burst and continuous sampling modes are supported. Input ranges are factory-configured as ±1V, ±100mV or ±10V for each of two input channel groups.

Four analog output channels provide software-selected output ranges of ±2.5V, ±5V or ±10V, and are accessed directly through dedicated control registers. A 16-Bit bidirectional digital port can be configured as two independent byte-wide ports.

An on-demand autocalibration feature determines offset and gain correction values for each input and output channel, and the corrections are applied subsequently during normal operation. A selftest switching network routes output channels or calibration reference signals to the analog inputs, and permits board integrity to be verified by the host..

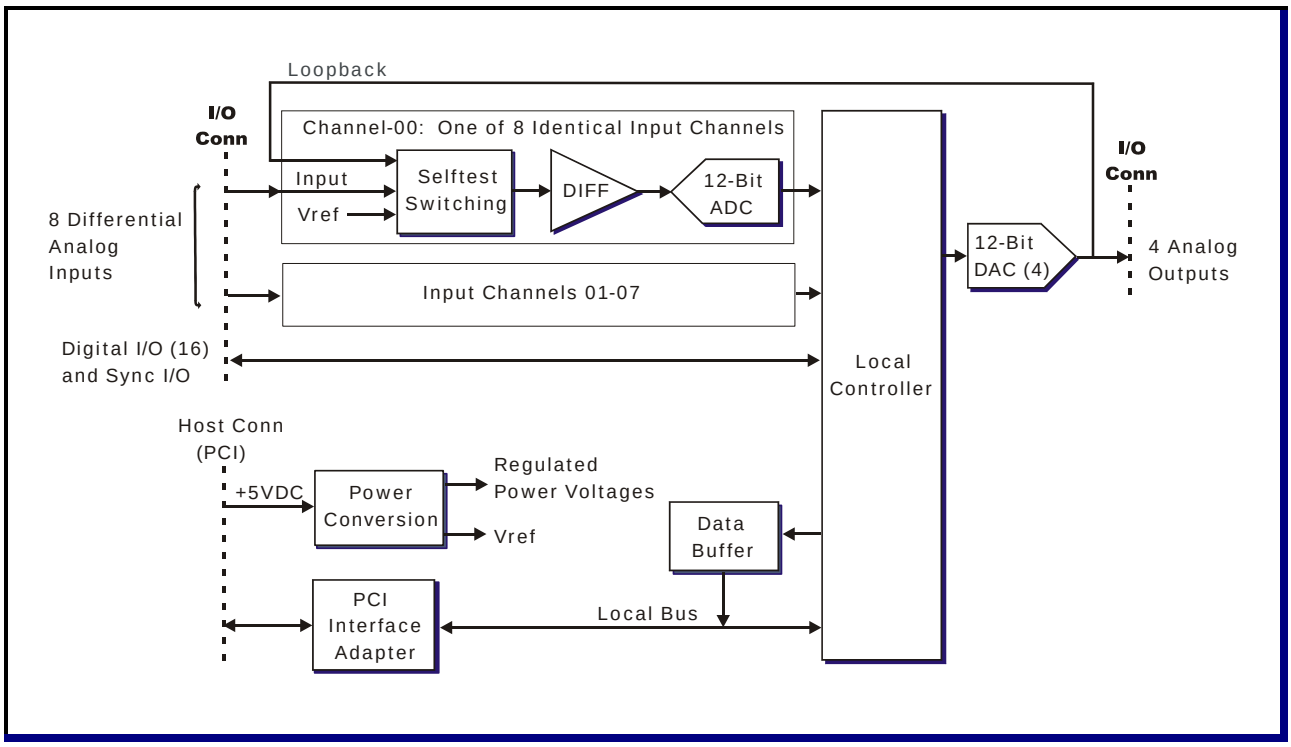

Figure 1. PMC-12AISS44AO4; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density dual-ribbon 80-pin connector. Power requirements consist of +5 VDC in compliance with the PCI specification, and analog power voltages are generated internally. All operational parameters are software configurable. Operation over the specified temperature range is achieved with conventional convection cooling.

PERFORMANCE SPECIFICATIONS

At +25 ^{O}C, with specified operating voltages

Analog Input Characteristics:

Configuration:	Eight differential analog input channels; Dedicated 12-Bit ADC per channel. Optional 4-Channel version available.
Voltage Ranges:	Two channel groups, each factory configured as ±100mV, ±1V or ±10V fullscale.
Input Impedance:	20 Megohms Line-Line in parallel with 40pF, typical.
Bias Current:	50 nanoamps maximum, all ranges.
Crosstalk Rejection:	70dB typical, DC-500kHz.
Signal/Noise Ratio (SNR):	±1V, ±10V Ranges: 70dB, ±100mVRange: 65dB; typical. (10 Hz to specified small-signal bandwidth. Signal = Fullscale-0.3dB).
Common Mode Rejection:	±1V, ±10V Ranges: 85dB, ±100mV Range: 95dB. Typical, DC-100Hz, CMV = ±11V, Vin = Zero.
Overvoltage Protection:	±40 Volts with power removed; ±25V with power applied.

Analog Input Transfer Characteristics:

Resolution:	12 Bits (0.0244 percent of FSR).		
Maximum Sample Rate:	2.0 MSPS per channel.		
Sampling Mode::	Simultaneous; 1 through 8 channels.		
DC Accuracy: (Maximum composite error after autocalibration)	Range	Midscale Accuracy	Fullscale Accuracy
	±10V	± 7 mV	±25mV
	±1V	± 2 mV	± 8mV
	±100mV	± 1 mV	± 3mV
Small-Signal Bandwidth:	DC to 900kHz, all ranges. 3dB typical.		
Settling Time (0.01%):	2.3us, all ranges, typical		
Power Bandwidth; -3dB	900kHz from 0Vp-p to 4Vp-p. 220kHz at 20Vp-p. 3dB typical.		
Integral Nonlinearity:	±0.035 percent FSR.		
Differential Nonlinearity:	±0.030 percent FSR.		

Analog Input Operating Modes and Controls

Input Data Buffer:	64K-sample FIFO.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock.
Sampling Modes:	Continuous sampling, and triggered burst.
Internal Rate Generator:	Programmable from 488-2,000,000 sample clocks per second. Divides 32MHz master clock to sample rate.
External Clock I/O:	TTL, bidirectional. Zero to 2,000,000 sample clocks per second.
Input Data Format:	Selectable as offset binary or as two's complement. All channels tagged.

Analog Output Characteristics:

Configuration:	Four single-ended output channels.
Voltage Ranges:	±10, ±5 or ±2.5 Volts; Software-selectable; Independent of analog input ranges.
Output Resistance:	1.0 Ohm maximum.
Output protection:	Withstands sustained short-circuiting to ground.
Load Current:	Zero to ±5ma per channel.
Load Capacitance:	Stable with any load capacitance.
Noise:	2.0mV-RMS, 10Hz-100KHz typical.
Glitch Impulse:	5 LSB-nSec typical, all ranges.

Analog Output Transfer Characteristics:

Resolution:	12 Bits (0.0244 percent of FSR)		
Output Clocking:	Direct register access. Outputs can update immediately upon receiving each new value from the bus, or can update synchronously from an internal or external clock. Maximum practical clocking rate is 400KSPS per channel.		
DC Accuracy:	Range	Midscale Accuracy	±Fullscale Accuracy
(Max error, no-load)	±10V	±10mV	±35mV
	±5V	±4mV	±18mV
	±2.5V	±2mV	±10mV
Settling Time:	4us to 1-LSB, typical with 50-percent fullscale step, no-load.		
Crosstalk Rejection:	65 dB minimum, DC-10 kHz.		
Integral Nonlinearity:	±0.04 percent of FSR, maximum.		
Differential Nonlinearity:	±0.03 percent of FSR, maximum.		

Digital I/O Port:

16-Bit bidirectional I/O port. Standard TTL levels. Direct register Access. Byte or word configuration.
20 mA loading when configured as an output port. 0.1 mA source when configured as inputs.

PCI Compatibility:

Conforms to PCI Specification 2.3, D32 read/write, 33MHz, universal (5V/3.3V) signaling,
Supports "plug-n-play" initialization,
Provides one multifunction interrupt,
Supports DMA data transfers in two channels as bus master in block mode or demand mode.

Power Requirements

+5VDC ±0.25 VDC at 1.5 Amp maximum, 1.1 Amp typical.

Maximum Power Dissipation: Side-1: 6.5 Watts. Side 2: 1.0 Watt.

PHYSICAL PARAMETERS

Mechanical Characteristics

Height: 13.5 mm (0.53 in)
Depth: 149.0 mm (5.87 in)
Width: 74.0 mm (2.91 in)

Environmental Specifications

Ambient Temperature Range:	Operating 0 to +65 Degrees Celsius inlet air: Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

ORDERING INFORMATION

Specify the basic product model number followed by an option suffix "-A-B-C-D", as indicated below. For example, model number PMC-12AISS44AO4-8-64K-4-LH describes a board with eight input channels, four output channels, a 64 Ksample data buffer, four ±100mV inputs and four ±1V inputs.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	**8 Input Channels**	**A = 8**
	4 Input Channels	**A = 4**
Buffer Size	**64 Ksamples**	**B = 64K**
Analog Outputs	**Four Analog Outputs**	**C = 4**
	No Analog Outputs	**C = 0**
Input Ranges	**Group-A and Group-B = ±100mV**	**D=LL**
	Group-A = ±100mV; Group-B = ±1V	**D=LH**
	Group-A and Group-B = ±1V	**D=HH**
	Group-A = ±100mV; Group-B = ±10V	**D=LV**
	Group-A = ±10V; Group-B = ±10V	**D=VV**

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Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	OUTPUT RTN
2	ANA OUT 00
3	OUTPUT RTN
4	ANA OUT 01
5	OUTPUT RTN
6	ANA OUT 02
7	OUTPUT RTN
8	ANA OUT 03
9	INPUT RTN
10	INPUT RTN
11	INP00 LO *
12	INP00 HI *
13	INPUT RTN
14	INPUT RTN
15	INP01 LO *
16	INP01 HI *
17	INPUT RTN
18	INPUT RTN
19	INP02 LO **
20	INP02 HI **
21	INPUT RTN
22	INPUT RTN
23	INP03 LO **
24	INP03 HI **
25	INPUT RTN
26	INPUT RTN
27	INP04 LO *
28	INP04 HI *
29	INPUT RTN
30	INPUT RTN
31	INP05 LO *
32	INP05 HI *
33	INPUT RTN
34	INPUT RTN
35	INP06 LO **
36	INP06 HI **
37	INPUT RTN
38	INPUT RTN
39	INP07 LO **
40	INP07 HI **

ROW-B	
PIN	SIGNAL
1	DIGITAL RTN
2	DIO 00
3	DIGITAL RTN
4	DIO 01
5	DIGITAL RTN
6	DIO 02
7	DIGITAL RTN
8	DIO 03
9	DIGITAL RTN
10	DIO 04
11	DIGITAL RTN
12	DIO 05
13	DIGITAL RTN
14	DIO 06
15	DIGITAL RTN
16	DIO 07
17	DIGITAL RTN
18	DIO 08
19	DIGITAL RTN
20	DIO 09
21	DIGITAL RTN
22	DIO 10
23	DIGITAL RTN
24	DIO 11
25	DIGITAL RTN
26	DIO 12
27	DIGITAL RTN
28	DIO 13
29	DIGITAL RTN
30	DIO 14
31	DIGITAL RTN
32	DIO 15
33	VTEST RTN
34	VTEST
35	DIGITAL RTN
36	OUTPUT CLK I/O
37	DIGITAL RTN
38	INPUT TRIG I/O
39	DIGITAL RTN
40	INPUT CLK I/O

* Input Group-A. ** Input Group-B.

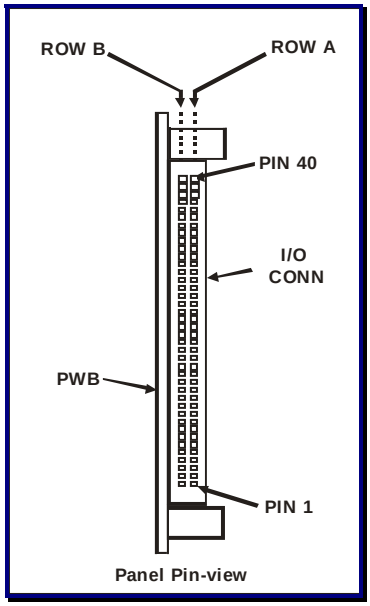

Figure 2. System Input Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent **P50E-080-S-TG,** or equivalent.