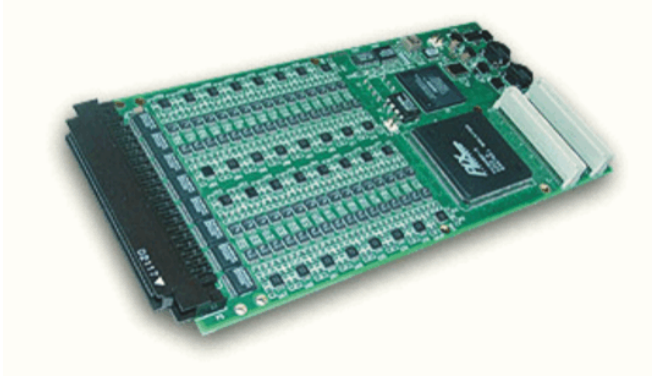
General Standards Corporation

High Performance Bus Interface Solutions

PMC-16AI64SSA

64-Channel, 16-Bit Simultaneous Sampling PMC Analog Input Board

With 200 KSPS Sample Rate per Channel



Features

- **64 Analog Inputs with Dedicated 200KSPS 16-Bit ADC per Channel**
- **True Simultaneous Sampling of all Inputs; Minimum Data Skew**
- **Sampling Rates to 200 KSPS per Channel (12.8 MSPS Aggregate Rate)**
- 64 Single-Ended Input Channels; Optional 32-Channel Configuration Available
- Selectable Differential Processing Simulates Differential Operation of Channel Pairs
- Input Ranges: ±10V, ±5V, ±2.5V, 0/+5V, 0/+10V; Software-Selectable
- Hardware Sync I/O for Multiboard Operation
- 256-Ksample FIFO Data Buffer
- Selectable Data Packing Supported by Sync Marker
- 2-Channel DMA Engine Supports Block-Mode and Demand-Mode Transfers
- Sampling Controlled by Internal Rate Generator, by Software Trigger, or Externally
- Internal Autocalibration of all Channels; On-Demand
- Completely Software-Configurable; No Field Jumpers
- Auxiliary PXI Triggering Port Available through P1, P2.
- Conforms to PCI Specification Revision 2.3, with Universal 5V/3.3V Signaling
- Single-width PMC Form Factor, with Integral EMI Shield

Typical Applications

✓ Analog Event Capture	✓ Industrial Robotics	✓ Acoustic Sensor Arrays
✓ Dynamic Test Systems	✓ Biometric Signal Analysis	✓ Vehicle Collision Testing

Rev-032505

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Functional Description

The 16-Bit PMC-16AI64SSA analog input board samples and digitizes 64 input channels simultaneously at rates up to 200,000 samples per second for each channel. Each input channel contains a dedicated 16-Bit sampling ADC. The resulting 16-bit sampled data is available to the PCI bus through a 256K-Sample FIFO buffer. The 16-Bit local data path can be packed into D32 PCI data longword format. All operational parameters are software configurable.

Inputs can be sampled in groups of 2, 4, 8, 16, 32 or 64 channels; or any single channel can be sampled continuously. The sample clock can be generated from an internal rate generator, or by software or external hardware. Input ranges are software-selectable as ±10V, ±5V or ±2.5V.

An on-demand autocalibration feature determines offset and gain correction values for each input channel, and the corrections are applied subsequently during acquisition. A selftest switching network routes calibration reference signals to each channel through internal selftest switches, and permits board integrity to be verified by the host..

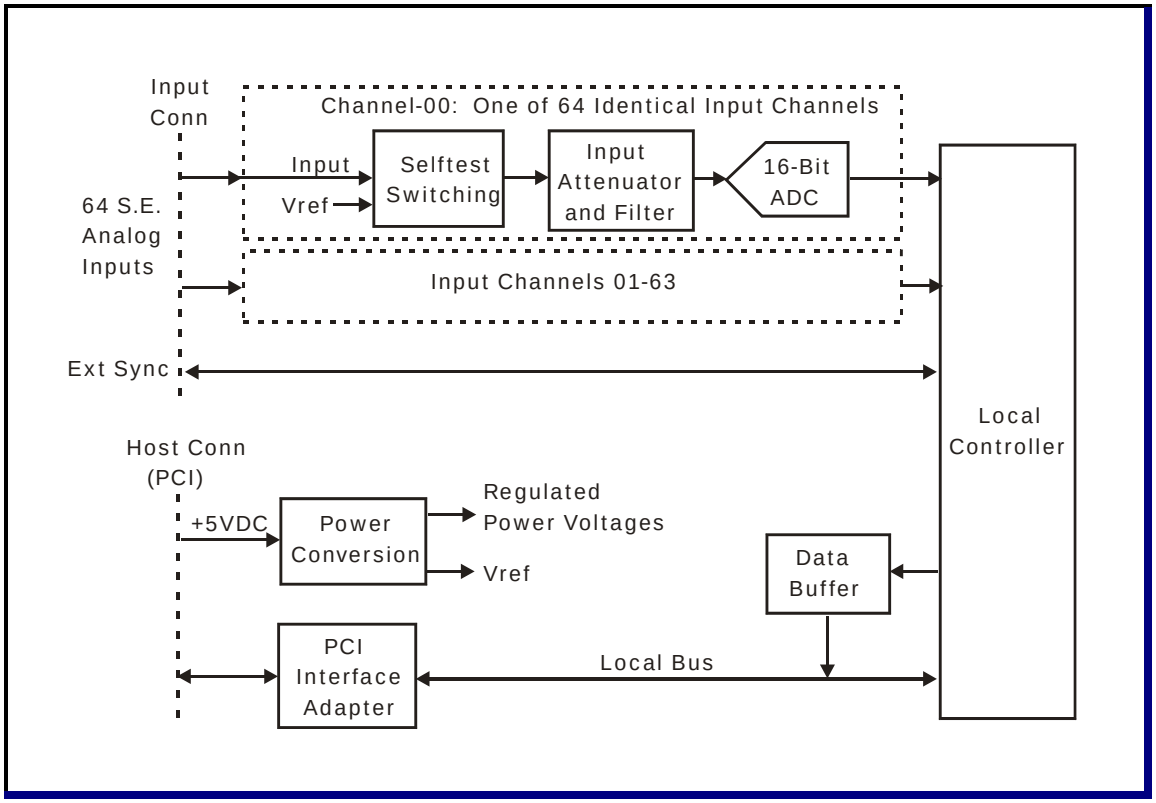

Figure 1. PMC-16AI64SSA; Functional Organization

This product is functionally compatible with the IEEE PCI local bus specification Revision 2.3, and supports the "plug-n-play" initialization concept. System connections are made at the front panel through a high-density 80-pin connector. Power requirements consist of +5 VDC, in compliance with the PCI specification, and operation over the specified temperature range is achieved with conventional convection cooling.

Performance Specifications

At +25 ^{O}C, with specified operating conditions

Input Characteristics:

Configuration:	64 single-ended analog input channels; Dedicated 16-Bit ADC per channel. Optional 32-Channel version available.
Voltage Ranges:	Software configurable as ±10V, ±5V, ±2.5V, 0/+5V or 0/+10V full scale
Input Impedance:	750 KOhms, typical.
Bias Current:	1ua maximum, ±2.5V range; 4ua maximum ±10V range
Crosstalk Rejection:	85dB typical, DC-50kHz
Input Noise, (0.01-50kHz):	0.5 mVRMS; typical, all ranges
Overvoltage Protection:	±40 Volts with power removed; ±25V with power applied.

Transfer Characteristics:

Resolution:	16 Bits (0.0015 percent of FSR)
Maximum Sample Rate:	200 KSPS per channel
Input Bandwidth (-3dB):	DC to 120 kHz typical
Channels per scan:	2, 4, 8, 16, 32 or 64 channels; or any single channel.

DC Accuracy: (Maximum composite error after autocalibration)

Range	Zero-Input *	Fullscale *
±10V	± 1.5mv	± 2.8mv
±5V	± 1.4mv	± 2.5mv
±2.5V	± 0.9mv	± 1.5mv
0/+10V	± 1.8mv	± 3.0mv
0/+5V	± 1.2mv	± 2.7mv

* Averaged values, referred to inputs. Typical values are approximately one-half the maximum values shown here.

Integral Nonlinearity:	±0.008 percent of FSR, maximum
Differential Nonlinearity:	±0.004 percent of FSR, maximum

Analog Input Operating Modes and Controls

Input Data Buffer:	256K-sample FIFO.
Sample Clock Sources:	Internal rate generator; External Hardware Sync I/O, Software clock.
Rate Generator:	Programmable from 0.01-200,000 sample clocks per second. Divides 30MHz master clock to sample rate. (Custom clock frequencies available).
External TTL Clock:	Bidirectional line; Zero to 200,000sample clocks per second.
Auxiliary Sync I/O:	Four independent bidirectional "PXI" lines in both PMC-P1/P2 and edge-board header; Zero to 200,000 sample clocks per second.
Input Data Format:	16-Bit data word plus single-bit Channel-00 tag. Format is selectable as offset binary or two's complement. Data packing replaces Channel-00 tag with a 32-Bit sync code.
Differential Processing:	Selectable processing options process input data as 63 pseudo-differential channels or as 32 full-differential channels.

PCI Compatibility:

Conforms to PCI Specification 2.3, with D32, 33MHz and universal (5/3.3 Volt) signaling
Single multifunction interrupt.
DMA transfers as bus master. Two DMA channels, block and demand transfer modes

Power Requirements

+5VDC ±0.2 VDC at 0.8 Amp maximum, 0.6 Amp typical.

Maximum Power Dissipation: Side-1: 3.5 Watts. Side 2: 0.5 Watt.

Physical Parameters

Mechanical Characteristics

Height:	13.5 mm (0.53 in)
Depth:	149.0 mm (5.87 in)
Width:	74.0 mm (2.91 in)
Shield:	Side-1 is protected by an EMI shield.

Environmental Specifications

Ambient Temperature Range:	Operating: 0 to +65 Degrees Celsius inlet air Storage: -40 to +85 Degrees Celsius
Relative Humidity:	Operating: 0 to 80%, non-condensing Storage: 0 to 95%, non-condensing
Altitude:	Operation to 10,000 ft.
Cooling:	Conventional convection cooling; 150 LFPM

Ordering Information

Specify the basic product model number followed by an option suffix "-A-B", as indicated below. For example, model number PMC-16AI64SSA-64-256K describes a board with 64 input channels and a 256 Ksample data buffer.

Optional Parameter	Value	Specify Option As:
Number of Input Channels	64 Channels	A = 64
	32 Channels	A = 32
Buffer Size	256 Ksamples	B = (Blank) or B = 256K

Note: Standard master clock frequency is 30MHz. Contact factory for custom frequencies.

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Table 1. System I/O Connector

ROW-A	
PIN	SIGNAL
1	INP00
2	INP01
3	INP02
4	INP03
5	INPUT RTN
6	INP04
7	INP05
8	INP06
9	INP07
10	INPUT RTN
11	INP08
12	INP09
13	INP10
14	INP11
15	INPUT RTN
16	INP12
17	INP13
18	INP14
19	INP15
20	INPUT RTN
21	INP16
22	INP17
23	INP18
24	INP19
25	INPUT RTN
26	INP20
27	INP21
28	INP22
29	INP23
30	INPUT RTN
31	INP24
32	INP25
33	INP26
34	INP27
35	INPUT RTN
36	INP28
37	INP29
38	INP30
39	INP31
40	INPUT RTN

ROW-B	
PIN	SIGNAL
1	INP32
2	INP33
3	INP34
4	INP35
5	INPUT RTN
6	INP36
7	INP37
8	INP38
9	INP39
10	INPUT RTN
11	INP40
12	INP41
13	INP42
14	INP43
15	INPUT RTN
16	INP44
17	INP45
18	INP46
19	INP47
20	INP48
21	INPUT RTN
22	INP49
23	INP50
24	INP51
25	INP52
26	INP53
27	INPUT RTN
28	INP54
29	INP55
30	INP56
31	INP57
32	INP58
33	INPUT RTN
34	INP59
35	INP60
36	INP61
37	INP62
38	INP63
39	SYNC I/O RTN
40	SYNC I/O

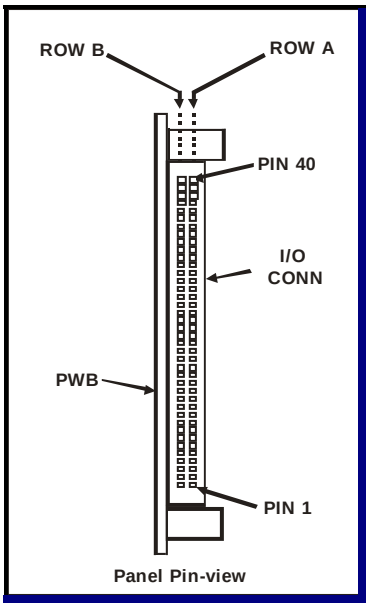

Figure 2. System Input Connector

System Mating Connector:

Standard 80-pin 0.050" dual-ribbon socket connector:

Robinson Nugent P50E-080-S-TG, or equivalent.