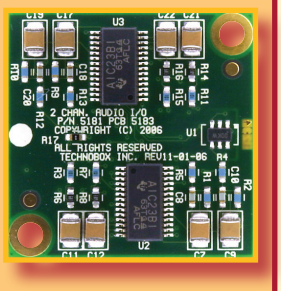
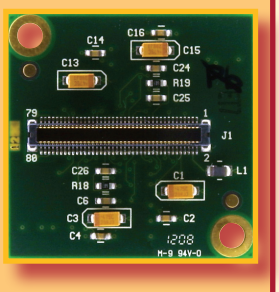
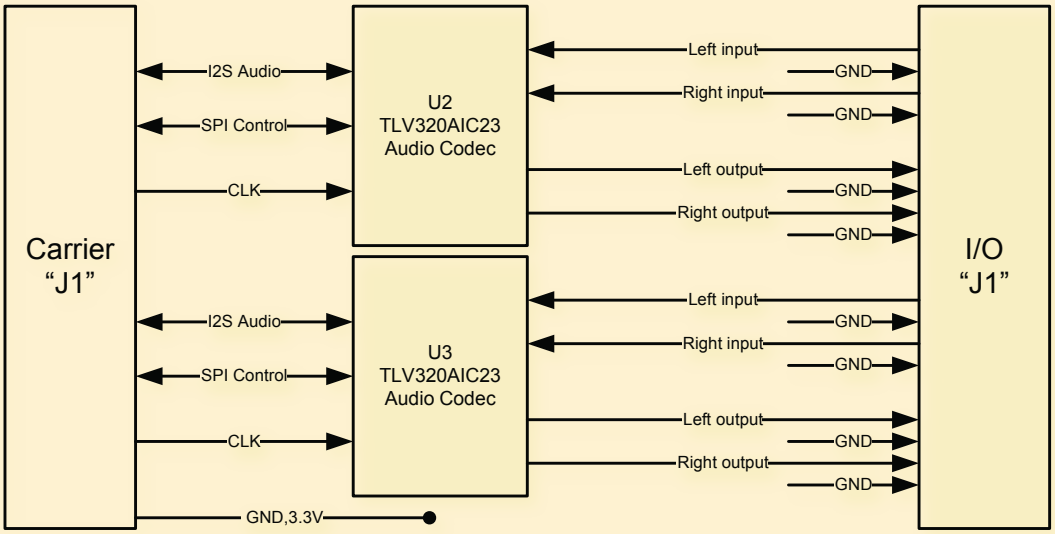
# Conversion Module

## Dual Stereo Codec - Line Level In / Out





**5181**




- **Analog input/output ECM**
- **TI TLV320AIC23 Audio Codec IC**
- **48 KHz or 96 KHz sample rates**
- **Oversampling rates of 256fs and 384fs**
- **2 channel of L/R line level input and output**
- **Capacitor coupled in-puts and outputs**
- **Inputs band pass filtered cutoff frequencies 2.6 Hz and 1.36 MHz**
- **Input voltage range 2Vrms**
- **Input gain adjustable -34.5 db to 12 db, 1.5 db steps, with mute**
- **Input Analog to digital converters, 90-dB SNR (A-weighted at 48 kHz)**
- **Outputs band pass filtered cutoff frequencies 4 Hz and 1.36 MHz**
- **Output voltage range 1Vrms, with mute**
- **Output digital to analog converters 100-dB SNR (A-weighted at 48 kHz)**
- **Powers up in the reset state**
- **On-board serial identification circuit.**
- **Industrial temperature range**
- **RoHS compliant**
- **Patented**

### Specifications

Temperature (Operating):
-40 to +85 degrees C

Temperature (Storage):
-55 to +100 degrees C

Altitude: Not Specified or Characterized. Typical similar equipment is at 15,000 ft.

Humidity (Operating/Storage):
5% to 90% non-condensing

Vibration: Not specified or Characterized

Shock: Not specified or Characterized

MTBF: Available on request

Weight: 3 grams

Power: TBD

### Ordering Information

5181: Dual Stereo Codec,
Line Level In / Out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140 Mount Holly Bypass
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The Technobox P/N 5181 ECM Audio I/O module uses the TI TLV320AIC23 audio codec to provide two channels of line input high resolution analog to digital conversion, along with 2 channels of high resolution digital to analog line drive output. Each input channel consists of two inputs a left and a right, and each output channel consists of two outputs left and right.

The inputs are capacitor coupled and band pass filtered with cutoff frequencies at 2.6 Hz and 1.36 MHz. The input voltage range is 2 Vrms and input gain is adjustable from -34.5 db to 12 db in 1.5 db steps, with mute. The Analog to digital converters are specified at 90-dB SNR (A-weighted at 48 kHz)

The outputs are capacitor coupled and high pass filtered with a cutoff frequencies at 4 Hz. The output voltage range is 1Vrms and drives 10K with 50pF loads, with mute. The Digital to analog converters are specified at 100-dB SNR (A-weighted at 48 kHz)

Sample rate of 48 KHz or 96 KHz for the input or output channels, with over-sampling rates of 256fs and 384fs.

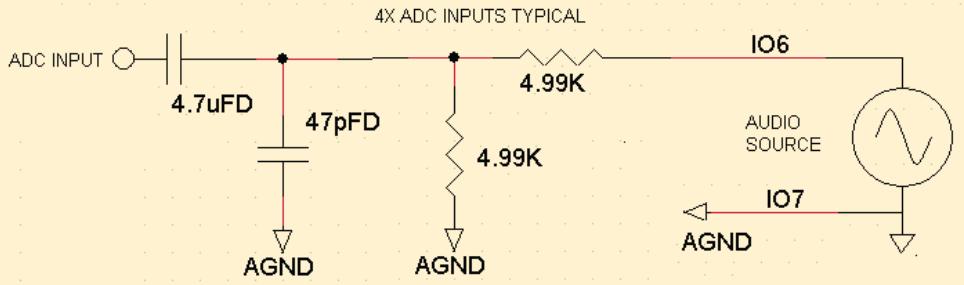
Eight grounds corresponding to the inputs and outputs ease wiring.

Powers up in the reset state.

Usage P/N 5181

Line input/output circuits: The 5181 provides line level outputs and inputs. Line level outputs typically can drive 5K ohms. A 8 ohm speaker is an example of an non-line level output..

Line input circuit: Inputs have a bandpass response of 2.6 Hz to 1.46 MHz 3 db. The input impedance of the ADC is a maximum of 10pF in parallel with 10K.




Line output circuit, Outputs have a high-pass filter cutoff of 4 Hz 3 db.

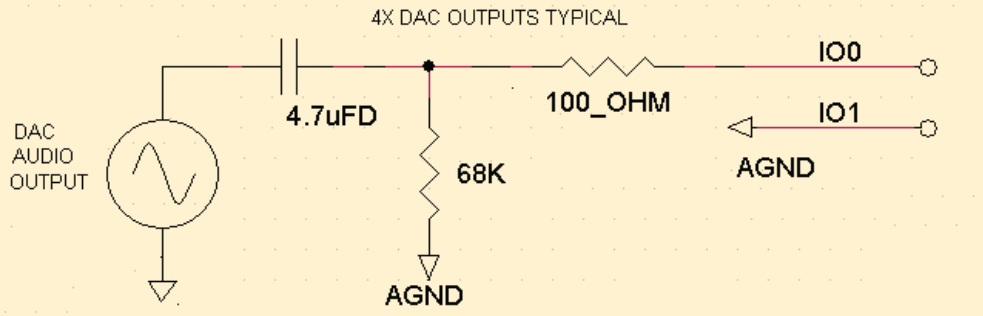



Figure 1 DAC output circuit

| User IO | J1 Pin number | J1 Direction | Description |
|---|---|---|---|
| IO0 | 16 | OUTPUT | U2 DAC voltage output left |
| IO1 | 18 | POWER | GND |
| IO2 | 28 | OUTPUT | U2 DAC voltage output right |
| IO3 | 30 | POWER | GND |
| IO4 | 52 | INPUT | U2 ADC voltage input left |
| IO5 | 54 | POWER | GND |
| IO6 | 64 | INPUT | U2 ADC voltage input right |
| IO7 | 66 | POWER | GND |
| IO8 | 65 | OUTPUT | U3 DAC voltage output left |
| IO9 | 63 | POWER | GND |
| IO10 | 53 | OUTPUT | U3 DAC voltage output right |
| IO11 | 51 | POWER | GND |
| IO12 | 29 | INPUT | U3 ADC voltage input left |
| IO13 | 27 | POWER | GND |
| IO14 | 17 | INPUT | U3 ADC voltage input right |
| IO15 | 15 | POWER | GND |

Table 1 User IO signal connections

| Carrier Data | J1 Pin number | J1 Direction | Description |
|---|---|---|---|
| DA0 | 10 | INPUT | U2, LRC in, Left Right Channel I2S signal for DACs |
| DA1 | 12 | INPUT | U2, data in I2S signal for DACs |
| DA2 | 22 | INPUT | U2, bit clock I2S signal for DACs and ADCs |
| DA3 | 24 | INPUT | U2, LRC, Left Right Channel I2S signal for ADCs |
| DA4 | 34 | OUTPUT | U2, data output I2S signal for ADCs. |
| DA5 | 36 | INPUT | U2, SPI signal CS chip select when low |
| DA6 | 46 | INPUT | U2, SPI signal SDIN serial data in |
| DA7 | 48 | INPUT | U2, SPI signal SCLK clock for serial data in |
| DA8 | 58 | INPUT | U2, Master clock 256 * Fsample |
| DA9 | 60 | N/C | No connection |
| DA10 | 70 | N/C | No connection |
| DA11 | 72 | N/C | No connection |
| DA12 | 71 | INPUT | U3, LRC in, Left Right Channel I2S signal for DACs |
| DA13 | 69 | INPUT | U3, data in I2S signal for DACs |
| DA14 | 59 | INPUT | U3, bit clock I2S signal for DACs and ADCs |
| DA15 | 57 | INPUT | U3, LRC, Left Right Channel I2S signal for ADCs |
| DA16 | 47 | OUTPUT | U3, data output I2S signal for ADCs. |
| DA17 | 45 | INPUT | U3, SPI signal CS chip select when low |
| DA18 | 35 | INPUT | U3, SPI signal SDIN serial data in |
| DA19 | 33 | INPUT | U3, SPI signal SCLK clock for serial data in |
| DA20 | 23 | INPUT | U3, Master clock 256 * Fsample |
| DA21 | 21 | N/C | No connection |
| DA22 | 11 | N/C | No connection |
| DA23 | 9 | N/C | No connection |
| DA24 | 40 | N/C | No connection |
| DA25 | 41 | N/C | No connection |
| DA26 | 42 | N/C | No connection |
| DA27 | 39 | N/C | No connection |

Table 2 Carrier DA signal connections

Each Audio codec has an I2S audio interface and a SPI interface to the carrier. In slave mode the I2S interface is driven by the carrier and provides the audio input and output data in a continuous stream. The SPI interface is used for configuration only.