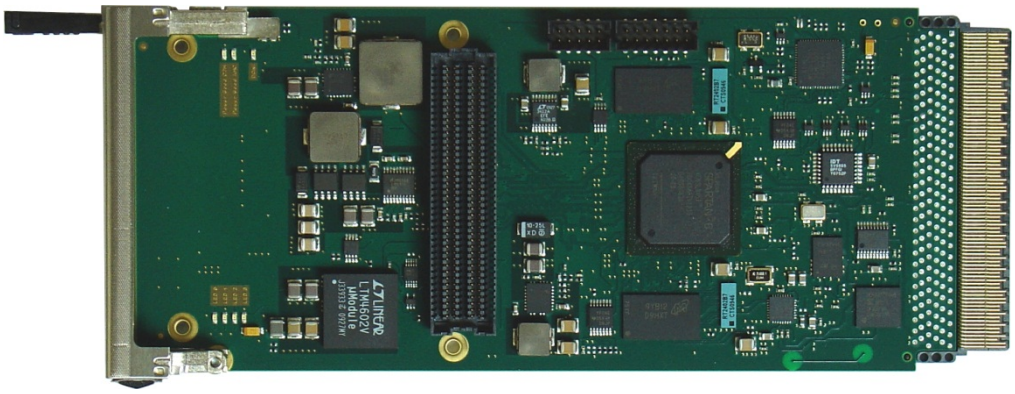
TAMC631 Spartan-6 AMC with FMC Module Slot



Application Information

The TAMC631 is a standard single Mid-Size or Full-Size AMC.1 Type 1 module providing a user configurable XC6SLX25T-2, XC6SLX75T-2, XC6SLX100T-2 or XC6SLX150T-2 Spartan-6 FPGA. The Spartan-6's PCIe Endpoint Block is connected to AMC port 4. The TAMC631 variants with XC6SLX75T, XC6SLX100T and XC6SLX150T FPGA also provide connections to AMC port 0 and 1.

For flexible front I/O solutions the TAMC631 provides a VITA 57.1 FMC Module slot with a low-pin count connector, allowing active and passive signal conditioning. All FMC I/O lines are directly connected to the FPGA, which maintains the flexibility of the SelectIO technology of the Spartan-6 FPGA. The low-pin count interface includes one multi-gigabit link.

The FPGA is connected to two banks of 128 Mbytes, 16 bit wide DDR3 SDRAM. The SDRAM-interface uses the hardwired internal Memory Controller Blocks of the Spartan-6.

The FPGA is configured by a platform flash which is programmable via a JTAG header. The JTAG header also supports readback and on-chip debugging of the FPGA design (using Xilinx "ChipScope"). An SPI-EEPROM can be used as alternative configuration source or for user data storage. The TAMC631 is delivered with blank configuration devices.

A programmable clock generator (5 KHz – 500 MHz) supplies up to three different clock frequencies to the FPGA. The clock generator settings are programmable via JTAG and are stored in an EEPROM. In addition two differential reference clocks are available from the FMC slot to the FPGA.

User applications for the TAMC631 with XC6SLX25T-2 and XC6SLX75T-2 FPGA can be developed using the design software ISE WebPACK which can be downloaded free of charge from www.xilinx.com. The larger FPGA densities require a full licensed ISE Design Suite.

The Engineering Documentation TAMC631-ED includes all information needed for customer specific FPGA programming. The FPGA Development Kit TAMC631-FDK includes the engineering documentation, ucf-files with all necessary pin assignments and basic timing constraints, and a well-documented VHDL example application. This example application is called TPLD001 (Tews Programmable Logic Design) and covers the main functionalities of the TAMC631 like DMA capable PCIe endpoint with interrupt support, register mapping, DDR3 memory access and basic I/O to the FMC slot. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream. It is the basis for fast and reliable customer application development, and can significantly reduce time to market.

Software support for the TPLD001 is available for all major operating systems.

Please note: The TPLD001 requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).

In-circuit programming and debugging of the FPGA design (e.g. using Xilinx "ChipScope") is supported. The Program and Debug Box TA900 allows access to the module while it is inserted in a system. It provides access to the module's JTAG Chain, the UART of the on-board Module Management Controller (MMC) and to two user pins of the Spartan-6 FPGA. If a UART core is implemented in the FPGA, serial communication via the TA900 is possible.

The TA900 can be accessed by USB 2.0 and by a 14-pin JTAG Header (e.g. for connecting a Xilinx Platform Cable).

For First-Time-Buyers the TA900 and the TAMC631-ED or TAMC631-FDK is recommended.

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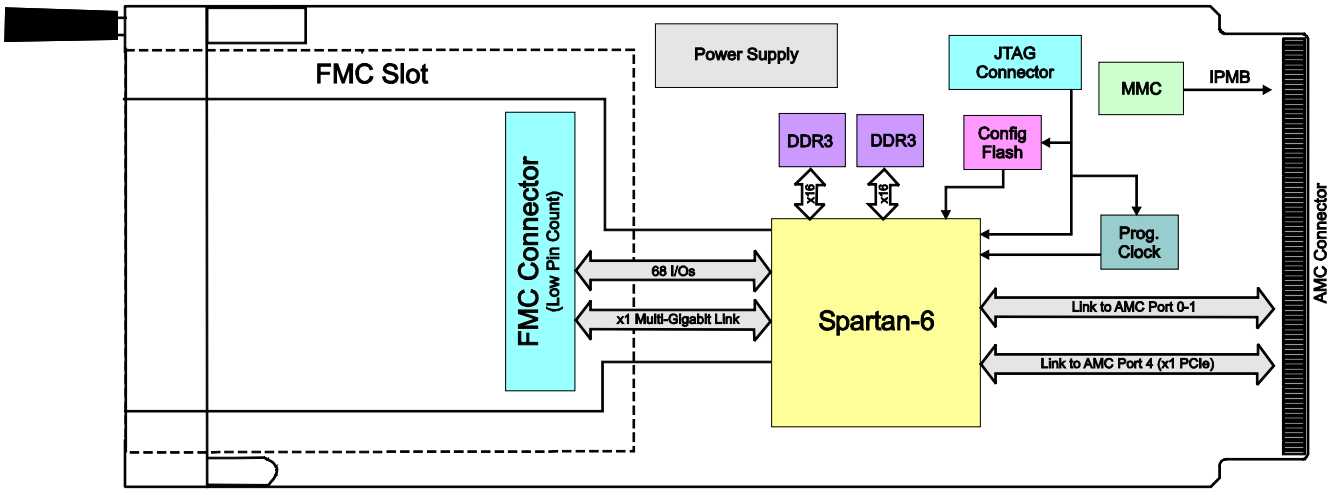
TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Technical Information

- Form Factor: PICMG AMC.0 R2.0Module
  - Board size: 180.6 mm x 73.5 mm
  - Single width
  - Mid-Size or Full-Size front panel
- PCIe x1 port (AMC.1 Type 1 compliant)
  - Optional connection to AMC port 0 & 1 (not for XC6SLX25T)
- IPMI V1.5 support
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red Power Good LED (LED1)
  - Green FPGA DONE LED (LED2)
- Spartan-6 FPGA
  - Xilinx XC6SLX25T/75T/100T/150T-2
- Flash device is programmable via JTAG
- FPGA clock options:
  - Programmable clock generator (5 KHz – 500 MHz), three clock outputs connected to FPGA
  - Two differential reference clocks from FMC slot
- 2x DDR3 SDRAM bank, 64M x 16 (128 MB) each
- 64 Mbit SPI-EEPROM
- VITA 57.1 FMC slot (low pin count)
  - 68 single-ended or 34 differential I/O lines
  - 2 differential reference clocks
  - x1 multi-gigabit link
  - V_{ADJ} = 1.2 – 3.3 Volt
- Operating temperature -40°C to +85°C
- MTBF (MIL-HDBK217F/FN2 G_B 20°C)
  TAMC631: 260 000 h



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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com

Order Information

RoHS Compliant

TAMC631-10R	Spartan-6 FPGA Module, Single Mid-Size, XC6SLX25T-2, 256 MB DDR3, FMC Slot
TAMC631-11R	Spartan-6 FPGA Module, Single Full-Size, XC6SLX25T-2, 256 MB DDR3, FMC Slot
TAMC631-12R	Spartan-6 FPGA Module, Single Mid-Size, XC6SLX75T-2, 256 MB DDR3, FMC Slot
TAMC631-13R	Spartan-6 FPGA Module, Single Full-Size, XC6SLX75T-2, 256 MB DDR3, FMC Slot
TAMC631-14R	Spartan-6 FPGA Module, Single Mid-Size, XC6SLX100T-2, 256 MB DDR3, FMC Slot
TAMC631-15R	Spartan-6 FPGA Module, Single Full-Size, XC6SLX100T-2, 256 MB DDR3, FMC Slot
TAMC631-16R	Spartan-6 FPGA Module, Single Mid-Size, XC6SLX150T-2, 256 MB DDR3, FMC Slot
TAMC631-17R	Spartan-6 FPGA Module, Single Full-Size, XC6SLX150T-2, 256 MB DDR3, FMC Slot

Optional available on request:

- Faster FPGA speed grades

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TAMC631-DOC	User Manual
TAMC631-ED	Engineering Documentation for TAMC631, includes TAMC631-DOC, Data Sheets, Constraints Files
TAMC631-FDK	FPGA Development Kit for TAMC631, includes TPLD001 Example Design

Accessories

TA900-10R	Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable

Software

TDRV015-SW-25	Integrity Software Support (for the example design TPLD001 of the TAMC631-FDK)
TDRV015-SW-42	VxWorks (Legacy and VxBus-Enabled) Software Support (for the example design TPLD001 of the TAMC631-FDK)
TDRV015-SW-65	Windows Software Support (for the example design TPLD001 of the TAMC631-FDK)
TDRV015-SW-72	LynxOS Software Support (for the example design TPLD001 of the TAMC631-FDK)
TDRV015-SW-82	Linux Software Support (for the example design TPLD001 of the TAMC631-FDK)
TDRV015-SW-95	QNX Software Support (for the example design TPLD001 of the TAMC631-FDK)

For other operating systems please contact TEWS.

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TEWS TECHNOLOGIES GmbH
Am Bahnhof 7 25469 Halstenbek, Germany
Phone: +49 (0) 4101 4058 0 Fax: +49 (0) 4101 4058 19
e-mail: info@tews.com www.tews.com