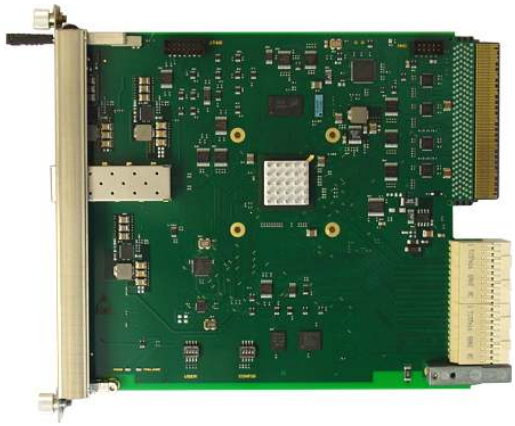
TAMC651 Spartan-6 FPGA AMC for MTCA.4 Rear-I/O



Application Information

The TAMC651 is a double Mid-Size or Full-Size AMC.1 Type 1 module according to MTCA.4 (MicroTCA Enhancements for Rear I/O and Precision Timing) and provides a user configurable Spartan-6 FPGA (XC6SLX45T-2 or XC6SLX100T-2).

The Spartan-6's integrated PCIe Endpoint Block is connected to AMC port 4.

AMC ports 12-15 (point-to-point) and AMC ports 17-20 (multi-drop) connect to FPGA I/O pins via on-board M-LVDS transceivers.

One of the Spartan-6 GTP transceiver utilizes an SFP interface available at the front plate. SFP support signals are available as FPGA I/O pins. Four FPGA controlled LEDs are also available at the front plate.

According to MTCA.4, the TAMC651 provides two 30-pair ADF connectors at the Zone 3 interface (Rear I/O).

The following I/O signals are available at the Zone 3 interface: 46 differential FPGA I/O lines (LVDS), 2 differential reference clock lines (LVDS), 2 Spartan-6 GTP transceivers. The differential FPGA I/O lines could also be used as single-ended I/O lines (FPGA bank supply for the Zone 3 I/O signals is 2.5V).

The TAMC651 provides a 128 Mbyte, 16 bit wide DDR3 SDRAM bank. The SDRAM-interface utilizes one of the internal hardwired Memory Controller Blocks of the Spartan-6 FPGA.

The FPGA is configured via a Xilinx platform flash which is programmable via a JTAG header. The JTAG header also supports readback and on-chip debugging of the FPGA design (e.g. using Xilinx "ChipScope"). A serial SPI-Flash can be used as alternative configuration data source or for user data storage.

The TAMC651 is shipped with blank configuration devices.

A programmable clock generator supplies differential clock lines to FPGA global clock pins, to an on-board clock crosspoint-switch and to the Spartan-6 GTP transceiver used for the SFP interface. The clock generator is programmable by the FPGA design.

The TAMC651 also provides a configurable clock crosspoint-switch. Clock inputs are: programmable clock generator output, FPGA clock output, AMC TCLKA and TCLKB. Two clock outputs are connected to FPGA global clock pins and two clock outputs are available as reference clocks at the Zone 3 interface.

User applications for the TAMC651 options with the XC6SLX45T-2 FPGA can be developed using the ISE WebPACK design software, which is available free of charge from www.xilinx.com. TAMC651 options with the XC6SLX100T-2 require a full licensed ISE Design Suite.

TEWS offers an FPGA Development Kit (TAMC651-FDK) which consists of a well documented basic example design. It includes an .ucf file with all necessary pin assignments and basic timing constraints. The example design covers certain functionalities of the TAMC651. It implements a DMA capable PCIe endpoint with interrupt support, register mapping and DDR3 memory access. It comes as a Xilinx ISE project with source code and as a ready-to-download bitstream.

Please note: The basic example design requires the Embedded Development Kit (EDK), which is part of the Embedded or System Edition of the ISE Design Suite from Xilinx (downloadable from www.xilinx.com, a 30 day evaluation license is available).

Software support for the basic design example of the TAMC651-FDK will be available for all major operating systems.

The TAMC651 can also be accessed via the TA900 program/debug box (USB 2.0 and/or 14-pin JTAG Header).

For First-Time-Buyers the TA900, the TAMC651-ED and TAMC651-FDK are recommended.

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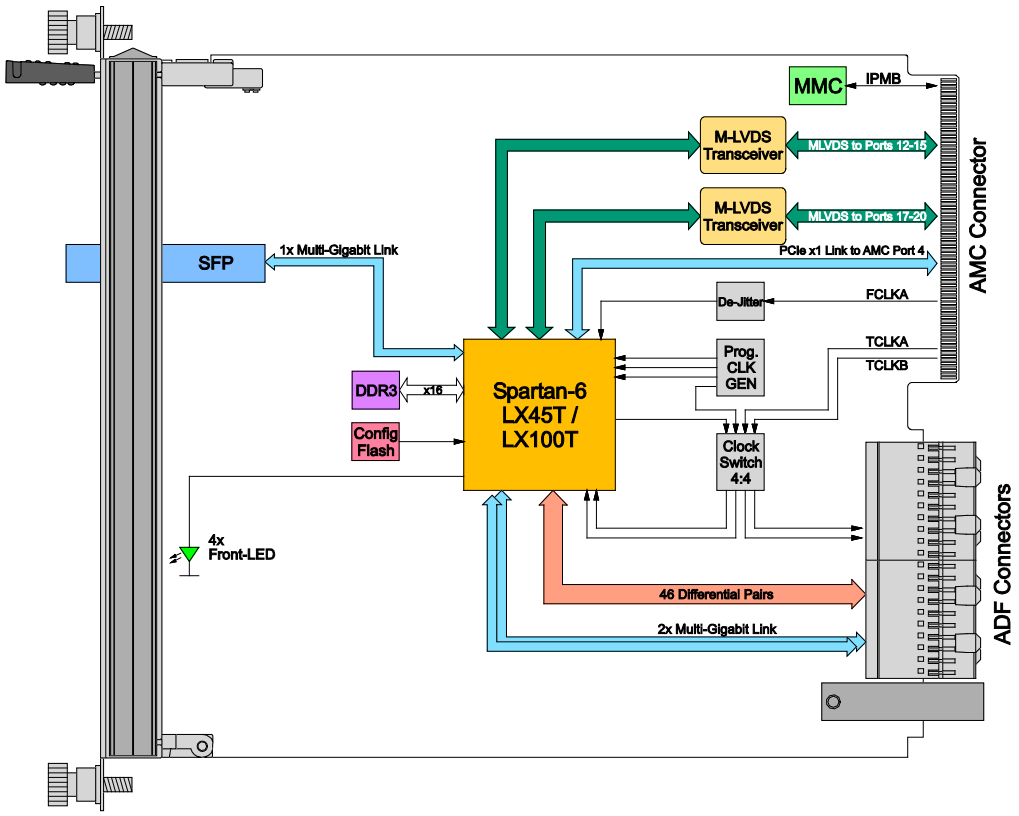
Technical Information

- Form Factor: PICMG AMC.0 Module
  - Double width
  - Mid-Size or Full-Size front panel
  - Front panel mechanics and Zone 3 interface according to MTCA.4
- PCIe x1 link (AMC.1 Type 1 compliant)
- M-LVDS transceivers for AMC ports 12-15 (point-to-point) and AMC ports 17-20 (multi-point)
- Spartan-6 FPGA
  - Xilinx XC6SLX45T-2 or XC6SLX100T-2
- FPGA configuration options
  - Xilinx Platform Flash
  - SPI serial Flash
  - JTAG Header
- DDR3 SDRAM bank, 64M x 16 (128 MB)
- Front Panel LEDs:
  - Blue Hot-Swap LED
  - Red LED (LED1)
  - Green LED (LED2)
  - 4x user programmable LED
- IPMI V1.5 support
- Programmable Clock Generator
  - 2 clock lines to FPGA
  - 1 clock line to SFP/GTP transceiver
  - 1 clock line to Clock Crosspoint-Switch
- Clock Crosspoint-Switch
  - Inputs: Programmable Clock Generator Clock Output, TCLKA, TCLKB, FPGA Clock output
  - Outputs: 2 clock lines to FPGA, 2 clock lines to Zone 3 interface
- MTCA.4 Zone 3 Interface I/O
  - 46 differential I/O lines (LVDS), could also be used as single-ended I/O lines (FPGA bank supply 2.5V)
  - 2 differential reference clocks
  - 2 Spartan-6 GTP transceivers (µRTM provides the GTP reference clocks)
- 1x SFP Interface at the front plate
- Zone 3 mechanical Key N = 1 (LVDS)



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Order Information

RoHS Compliant

TAMC651-10R	Spartan-6 FPGA Module, Single Mid-Size, MTCA.4 I/O, XC6SLX45T-2, 128 MB DDR3, 1 x SFP Port
TAMC651-11R	Spartan-6 FPGA Module, Single Full-Size, MTCA.4 I/O, XC6SLX45T-2, 128 MB DDR3, 1 x SFP Port
TAMC651-12R	Spartan-6 FPGA Module, Single Mid-Size, MTCA.4 I/O, XC6SLX100T-2, 128 MB DDR3, 1 x SFP Port
TAMC651-13R	Spartan-6 FPGA Module, Single Full-Size, MTCA.4 I/O, XC6SLX100T-2, 128 MB DDR3, 1 x SFP Port

Optional available on request:

- Faster FPGA speed grades

For the availability of non-RoHS compliant (leaded solder) products please contact TEWS.

Documentation

TAMC651-DOC	User Manual
TAMC651-ED	Engineering Documentation for TAMC651, includes TAMC651-DOC, Data Sheets, Constraints Files
TAMC651-FDK	FPGA Development Kit for TAMC651, includes TPLD004 Example Design

Accessories

TA900-10R	Program and Debug Box, USB, JTAG, 20pin FPC connector, including USB A-USB B and FPC Flexcable

Software

TDRV015-SW-25	Integrity Software Support (for the example design TPLD004 of the TAMC651-FDK)
TDRV015-SW-42	VxWorks (Legacy and VxBus-Enabled) Software Support (for the example design TPLD004 of the TAMC651-FDK)
TDRV015-SW-65	Windows Software Support (for the example design TPLD004 of the TAMC651-FDK)
TDRV015-SW-72	LynxOS Software Support (for the example design TPLD004 of the TAMC651-FDK)
TDRV015-SW-82	Linux Software Support (for the example design TPLD004 of the TAMC651-FDK)
TDRV015-SW-95	QNX Software Support (for the example design TPLD004 of the TAMC651-FDK)

For other operating systems please contact TEWS.

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